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Report Title

Final Report: Scalable Multiplexed Ion Trap Fabrication Using Ball Grid Arrays

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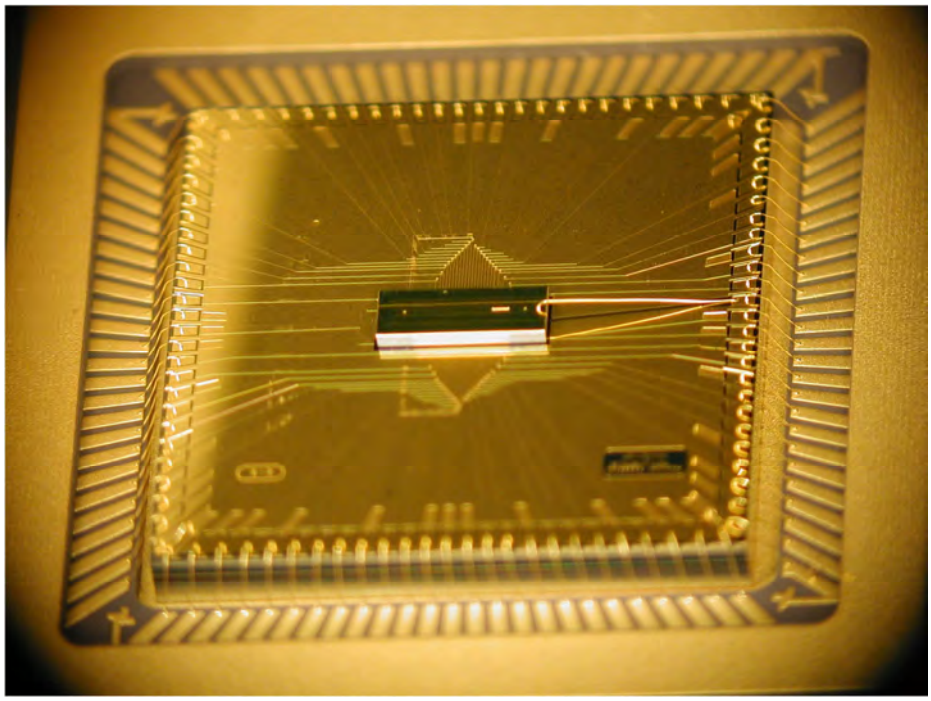


SMIT Ball Grid Array Final Report

October 1, 2014

Georgia Tech Research Institute

Honeywell International

Dan Youngner, Matthew Jungwirth, James Goeders, Thomas Ohnstein, Matt Marcus, Nicholas Guise, Jason Amini, Spencer Fallek, Curtis Volin, and Alexa Harter

Abstract

State-of-the art microfabricated ion traps for quantum information research have grown to incorporate upwards of a hundred control electrodes. In the typical architecture, a surface-electrode ion trap is fabricated on a thin chip that sits atop an industry standard CPGA carrier. To supply DC potentials for each electrode, pads on the CPGA are wirebonded to pads on the trap chip, while on-chip surface capacitors suppress pickup from the RF trapping fields. For large numbers of electrodes, the physical area taken up by these wirebonds and filter capacitors present significant constraints for ion trap design and operation. We report here on the development and successful testing of a new architecture for microfabricated ion traps, built around ball-grid array (BGA) connections and trench capacitors. In the BGA trap, through-substrate vias (TSVs) are used to bring electrical signals from the back side of the trap die to the top side. Gold-ball bump bonds connect the back side of the trap die to a separate interposer for signal routing from the CPGA carrier. Trench capacitors fabricated into the trap die eliminate the need for surface capacitors, reducing the trap die area by 30x. Wirebonds in the BGA architecture are moved to the interposer, leaving the surface of the trap chip fully unobstructed for laser access. Performance of the BGA trap as characterized with $^{40}Ca^{+}$ ions is comparable to or better than previous GTRI surface traps in terms of ion heating rate, axial mode stability, and dark lifetime for one and two trapped ions. We take advantage of the smaller trap dimensions to demonstrate improved single-qubit rotation rates through tight focusing of an addressing laser beam. We describe a proposed system of integrated micro-optics for addressing and detecting ions in a BGA trap array.

Table of Contents

1 Introduction

Trapped atomic ions are a leading platform in quantum information research, offering the advantages of precise optical manipulation and long qubit coherence times. One transport architecture proposed for scalable trapped-ion quantum computing[1] requires a complex system in which large numbers of ions are shuttled between many interaction zones for pairwise operations. Towards this goal, microfabrication techniques have enabled miniaturization of ion traps; recent surface electrode traps incorporate upwards of 100 control electrodes on a substrate chip of size 1 cm x 1 cm. However, further scalability of surface-electrode ion traps is currently limited by the wirebond density around the perimeter of the trap die and the surface area occupied by the capacitors used to suppress RF pickup on the control electrodes. In the typical architecture, a surface-electrode ion trap is fabricated on a thin chip that sits atop an industry standard ceramic pin-grid array (CPGA) carrier. To supply DC potentials for each electrode, pads on the CPGA are wirebonded to pads on the trap chip, while surface capacitors on the trap chip are used to filter out RF pickup. Already for existing traps with ~100 electrodes, the surface capacitors and bond pads consume >95% of the overall trap chip area, constraining the layout of electrode structures and DC/RF lead traces. Meanwhile, wirebonds must be carefully arranged to minimize obstructions to laser access, as the beams for trapping and qubit manipulation must interact with ions confined <100 μm above the chip surface.

For the BGA seedling, Georgia Tech Research Institute and Honeywell International collaborated to demonstrate a new architecture for microfabricated ion traps, built around ball-grid array (BGA) connections. The BGA trap mitigates scalability concerns related to the surface capacitors and wirebond connections, providing a flexible architecture for traps of increased complexity. The trapping electrodes on the top surface of the BGA trap are connected with through-substrate vias (TSVs) to pads on the back-side of the trap die. Gold-ball bump bonds then connect these back-side pads to a separate interposer for signal routing from the CPGA carrier. Trench capacitors fabricated into the trap die eliminate the need for surface capacitors, reducing the trap die area by 30x. With the wirebond connections relocated to the interposer, the surface of the trap chip remains unobstructed for laser access. Details of the BGA trap fabrication process are provided in Section 2.

We characterize the BGA trap by loading single and multiple $^{40}Ca^{+}$ ions. Performance of the trap is comparable to or better than previous GTRI surface traps in terms of ion heating rate, axial mode stability, and dark lifetime for one and two trapped ions. We take advantage of the reduced trap die size and improved optical access to demonstrate a speedup in single-qubit rotation rates through tight focusing of an addressing laser beam. Results from BGA ion trap testing are presented in Section 3.

In Section 4 we explore future possibilities for integrating micro-optics to address and detect ions in a BGA trap or array of BGA traps. We present details of a proposed scalable multiplexor system for single-ion addressing.

2 Fabrication

2.1 Overview

The trap used as the starting point for this investigation is the GTRI-designed "Gen-II" trap[2] shown in Figure 1.

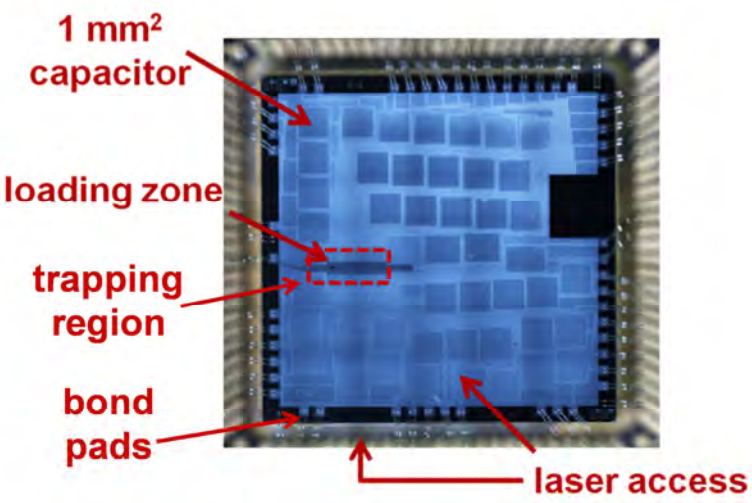


Figure 1: Photograph of the GTRI Gen-II trap.

The Gen-II traps are capable of trapping ions, but they have several less-than-ideal attributes, including:

1.) At ~1 cm x 1 cm, they are physically big devices.
2.) The trapping region of the die takes up only ~3% of the die's surface area. Roughly 97% of the die is taken up by capacitors and bond pads.
3.) Because of the large periphery (non-trap area) and large distance from the edge of the die to the center of the trap, it is difficult to focus a laser on an ion while maintaining a narrow beam waist. Large beam waists make it difficult to perform high-fidelity operations involving more than one ion.
4.) Much of the periphery of the die is blocked by bond wires. The obstructed view of the ions limits one's flexibility in performing quantum operations involving more than one ion.
5.) The traps are made from aluminum metal. Aluminum is prone to forming "hillocks" (crystalline protrusions) and to growing an oxide skin – both of which can be detrimental to trap operation.
6.) There is exposed SiO2 in the gaps between metal features. The SiO2 can accumulate quasi-mobile surface charge, which can contribute to unpredictable behavior.

While some of these undesired attributes have been addressed in subsequent GTRI trap designs, addressing them comprehensively was the focus of the BGA program.

The specific goals of the BGA program included:

1.) Designing and making segmented planar Paul traps that included all of the key features of the GTRI traps (electrode pitch, operating voltages, RF rails, etc.).
2.) Ensuring that the finished device would be compatible with GTRI's existing vacuum station, electronics, fixtures, and optics.
3.) Shrinking the area of the die to only the area required to produce trapping fields.
4.) Eliminating wire bonds from the perimeter of the trap, thereby opening the perimeter for optical access.
5.) Using a non-oxidizing metal such as gold for the trap surfaces.

To meet these goals, several new design and process features were developed, including:

1.) On-chip trench capacitors with a >100x reduction in die surface area compared to the 1 mm x 1 mm Gen-II capacitors.
2.) Through-substrate vias (TSVs) to bring electrical signals from the back-side of the die to the front-side.
3.) A re-entrant metallization profile that screens any trapped charge that might accrue on dielectric surfaces.
4.) A separate interposer beneath the trap die for signal routing.

Figure 2 shows how the Gen-II trap evolved to become the BGA trap. Shown in the upper right is a layout plot of the Gen-II trap in a 100-pin Kyocera CPGA (Ceramic Pin Grid Array) package. GTRI's test fixtures have been designed to accommodate the CPGA package. The upper left is a zoomed-in view of the trapping region of the die. The lower left shows the BGA ion trap. The electrode pitch and trapping electrodynamics of the BGA trap are designed to replicate the GTRI Microwave trap[3]. Importantly, the filter capacitors that take up much of the periphery of earlier GTRI designs have been shrunk and incorporated into the much smaller BGA version of the trap. The lower right figure shows an interposer and a BGA trap die mounted into the standard 100-pin CPGA package.

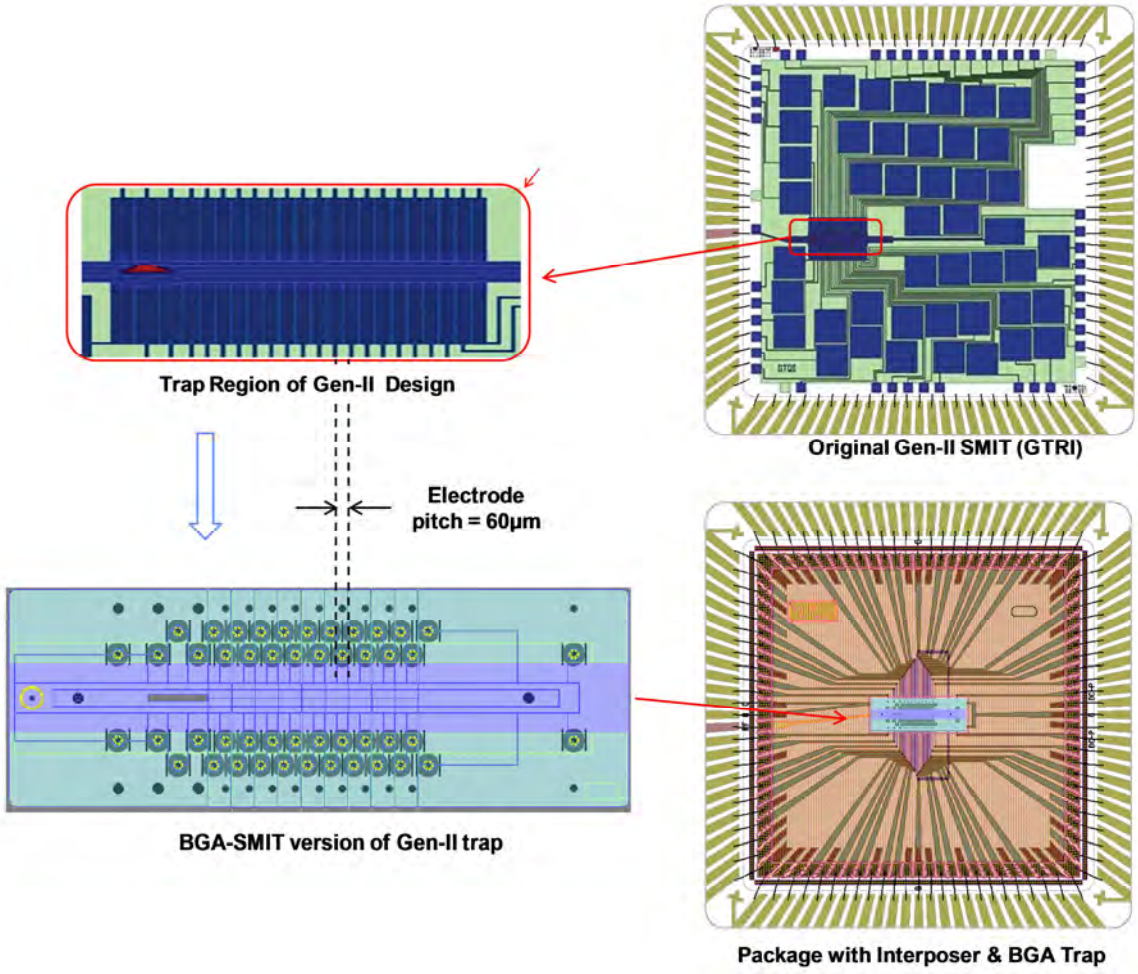


Figure 2: Evolution of a Gen-II trap (upper right) to a BGA trap (lower right).

Figure 3 shows some of the details of the BGA trap, including the loading slot, the TSVs, and the trench capacitors. There are 48 trench capacitors and 48 TSVs connected to a total of 48 DC electrodes. External digital-to-analog converters (DACs) provide independent signals to each electrode.

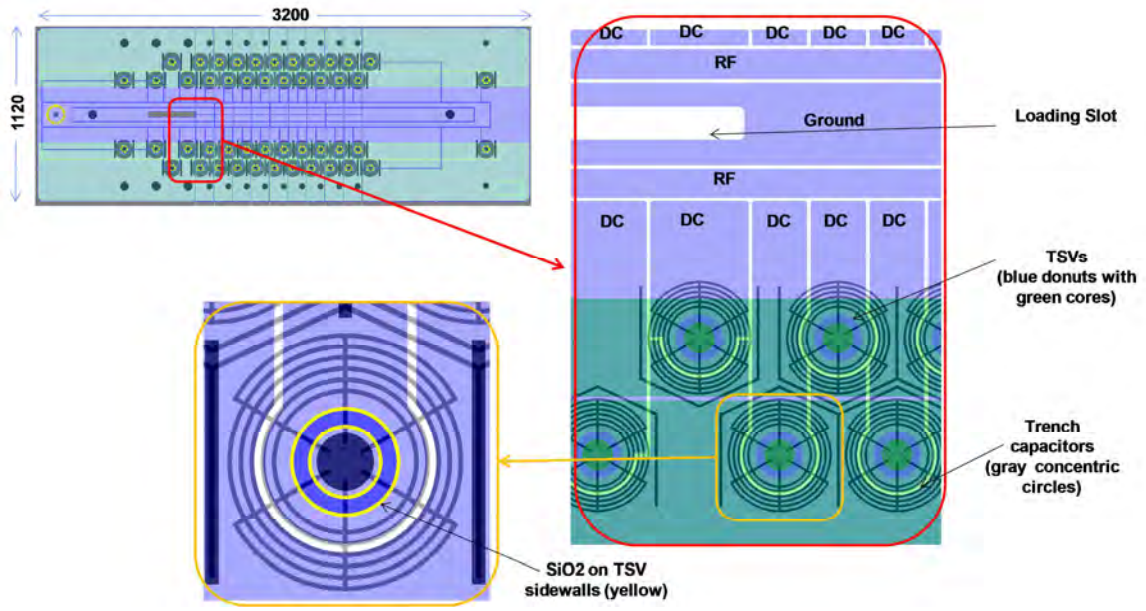


Figure 3: Entire trap die (upper left), closer view showing the loading slot, the TSVs, and the trench capacitors (right), and even closer view showing the SiO2 around the TSVs (lower left)

Figure 4 is a schematic cross section of the BGA trap. The drawing is not to scale, but it shows how all the key features (metal layers, trench capacitors, TSVs) are positioned relative to one another. It also shows an interposer that is solder-bonded to the bottom of the trap die, and a laser beam that is focused on a single ion trapped above the surface of the die.

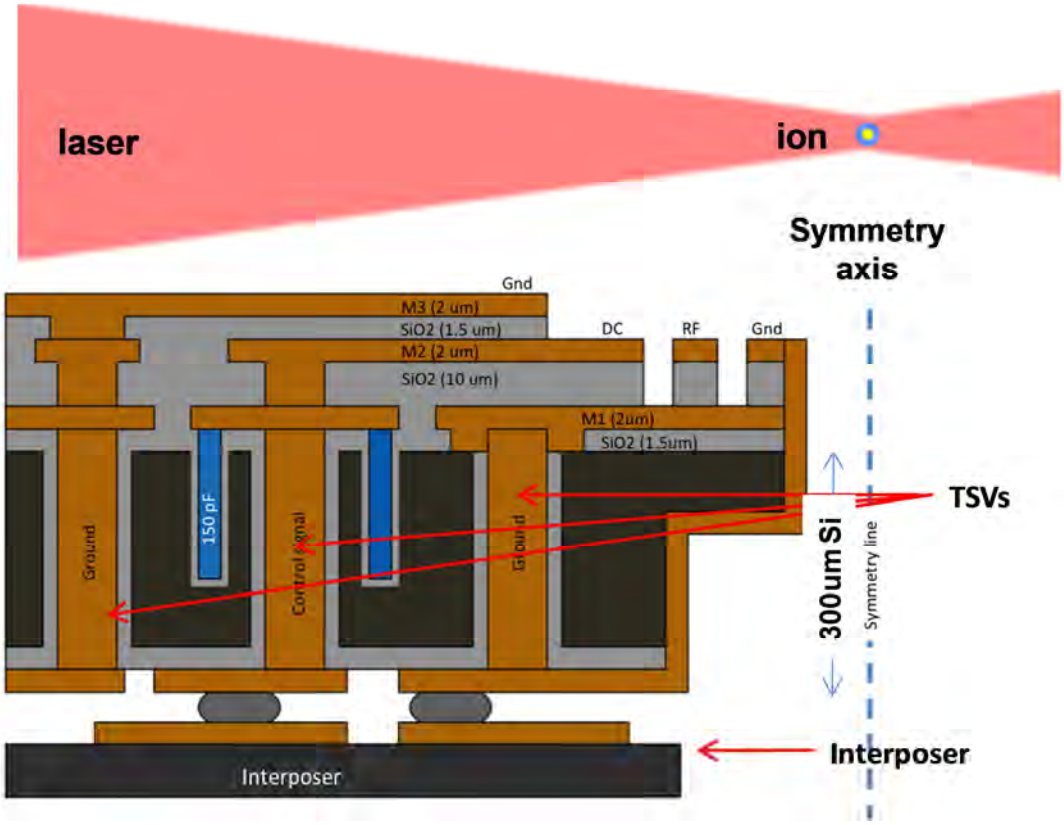


Figure 4: Schematic cross-section through a BGA trap.

Figure 5 is a layout plot of the interposer. The interposer is a 1 cm x 1 cm by 1.3 mm-thick piece of silicon with one layer of patterned metal on the top and one layer of blanket (unpatterned) metal on the bottom. Its main purpose is to make electrical connections from the package to the trap die. A slot is cut through the interposer to allow a flux of neutral atoms provided by an oven to travel from the back of the CPGA package, though a hole in the package, through a hole in the interposer, through a hole (loading slot) in the trap die, and up to the top surface of the trap.

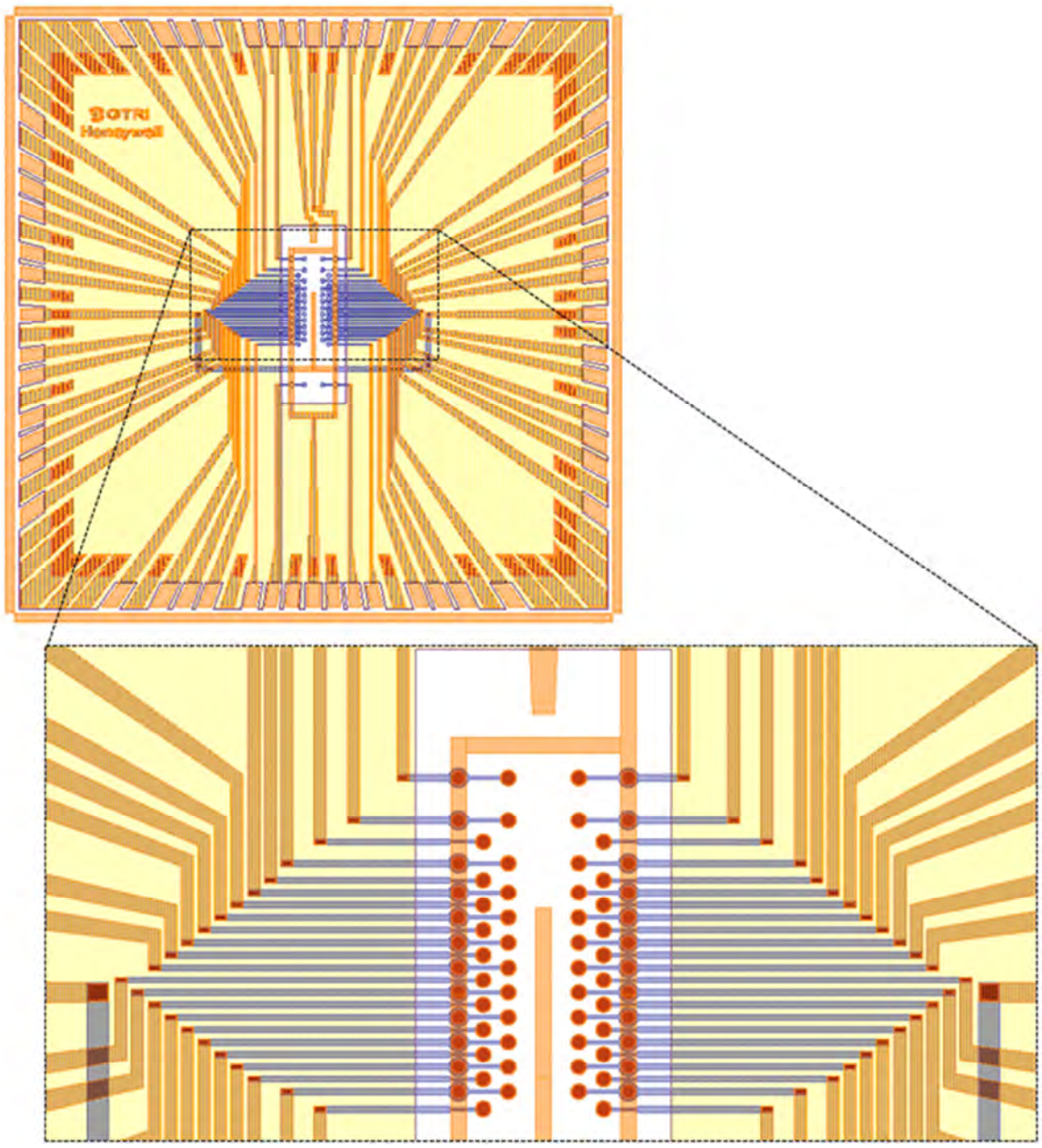


Figure 5: Interposer layout with inset showing connection pads under the BGA. The loading slot is not shown.

The process for making trap die, the process for making the interposer, and the process for assembling the trap and interposer into a Kyocera 100-pin CPGA are described in greater detail in section 2.2 below.

2.2 Processing Details

2.2.1 Trap Die Fabrication

The process for making the trap die has several key steps, including:

1.) Making Through-Substrate Vias (TSVs)
2.) Making trench capacitors
3.) Making ohmic contact to the silicon substrate and to polysilicon with a thin layer of platinum-silicide.
4.) Patterning 3 layers of gold on the top-side (the trapping side) of the trap wafer.
5.) Patterning 1 layer of gold on the back-side (the interposer side) of the trap wafer.
6.) Making loading slots and lining them with gold. Die singulation ("dicing") happens at the same time as the loading slots are being fabricated.

1.) Making Through-Substrate Vias (TSVs): The process for making the trap die begins with a 500 µm-thick p++ (heavily boron-doped) silicon wafer with a resistivity of ~0.001 – 0.005 Ωcm. The outlines for the TSVs are patterned with donut-shaped features and etched ~340 µm into the wafer using a Deep Reactive Ion Etch (DRIE) tool, as shown in Figure 6, step 1. The side and bottom walls of the TSVs are oxidized in a thermal oxidation furnace to a thickness of 1.5 µm (step 2). The trenches are filled with ~6 µm of highly conductive p++ polysilicon, completely sealing tops of the holes (step 3). A Chemical –Mechanical Polish (CMP) is performed from the front-side to expose the original bulk silicon wafer (step 4), and an additional thermal oxide layer is grown (not shown). Much later in the process (after all front-side metallization is complete), another CMP operation is performed – this time from the back of the wafer (step 5). The back-side CMP reduces the wafer thickness to 300 µm, and at the same time exposes the TSV "donut". Once the back-side CMP is complete the core of the donut (the TSV itself) is electrically isolated from the bulk silicon wafer. Figure 6 shows the complete process for forming the TSVs.

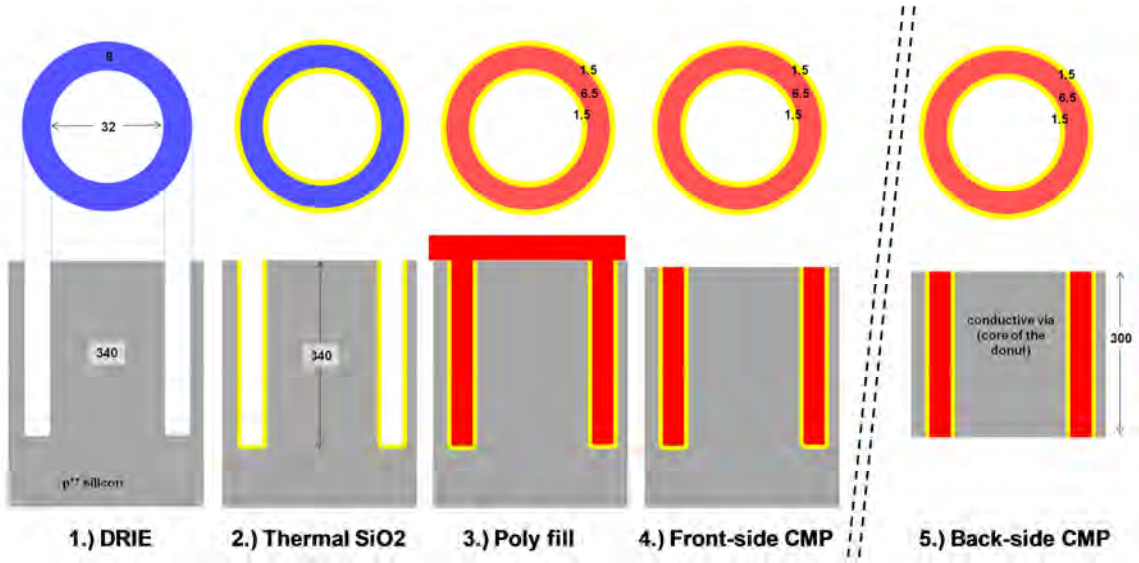


Figure 6: Process for making TSVs.

The TSV photomask resembles a tray full of donuts, with one donut for every DC electrode. Figure 7 shows scanning electron microscope (SEM) images of some of the TSVs after DRIE but before growing the 1.5 µm thermal SiO2 on the sidewalls of the donuts.

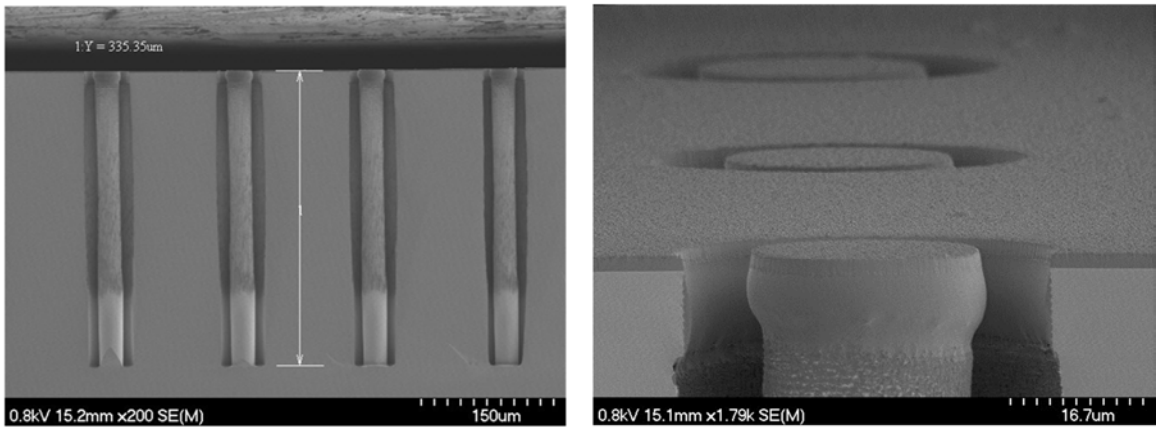


Figure 7: SEM images showing a cross-section (left) and a high-angle surface view of the "donut vias" after DRIE, but before the first thermal oxidation.

The left-hand side of Figure 8 is the same cross-section as the left-hand side of Figure 7, but has been cropped to show where the back-side grind-and-polish ends (step 5). The right-hand side of Figure 8 shows SEM images of the front and back of a TSV following polysilicon fill and CMP. The TSV resistances are all 40 +/- 2 Ω. The breakdown voltages of the TSVs were all measured to be >380 volts (the limits of the equipment used for the test). The breakdown measurements are not made until after 1st metal had been patterned. Once 1st metal covers the die, however, the surface is so planar that it becomes difficult to see which parts of the structure are being tested. The lower right-hand side of Figure 8 shows electrically which parts of the structure are used in the breakdown tests. The breakdown voltage across the gaps shown by the 2 red dots was always greater than 380 volts.

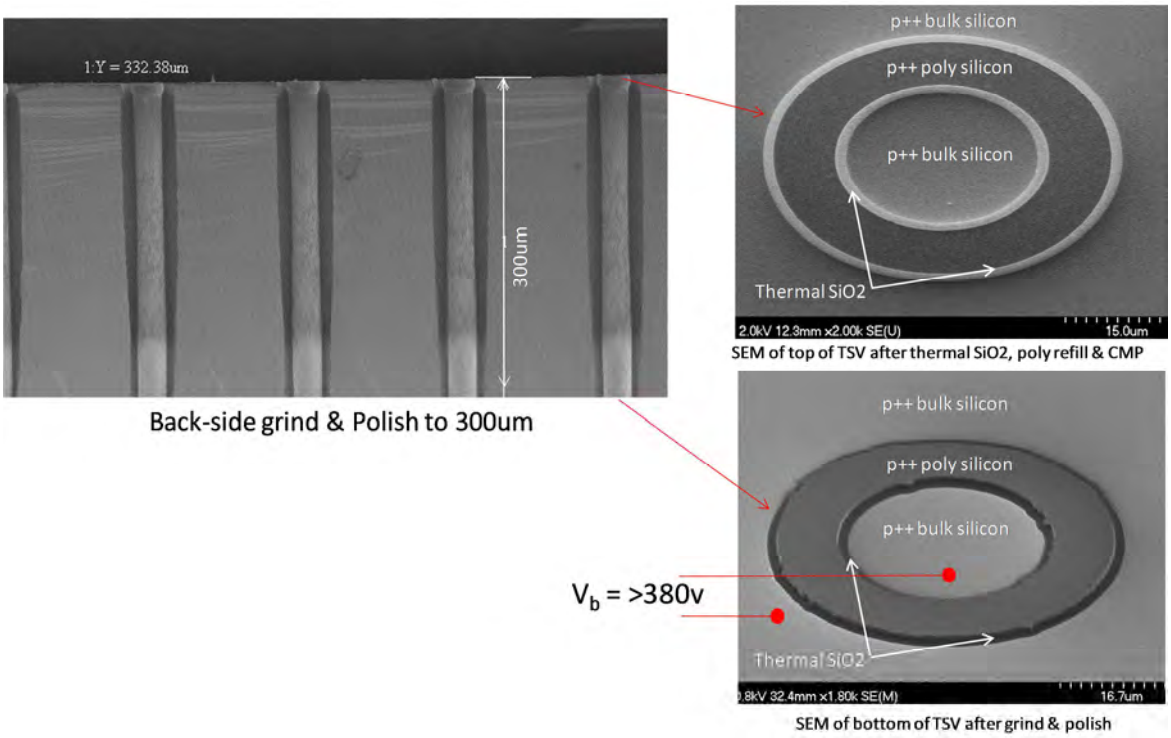


Figure 8: SEM images of the TSVs after CMP (left), after front-side CMP (top right), and after back-side CMP (bottom right).

2.) Making Trench Capacitors.

The trench capacitors are made using a 5-step process:

1.) DRIEing (Deep Reactive Ion Etching) interdigitated finger-like trenches, arranged in concentric rings around the TSVs, which extend 55-70 µm into the silicon wafer.
2.) Growing a 600-900 angstrom thermal oxide on the sidewalls of the trenches.
3.) Filling those trenches with p++ (heavily boron-doped) poly silicon.
4.) CMPing the surface of the wafer until the bulk silicon wafer has been exposed.
5.) Growing 0.5 µm of thermal SiO2 to consume CMP damage.

Figure 9 through Figure 12 show the trench capacitors at various stages of processing.

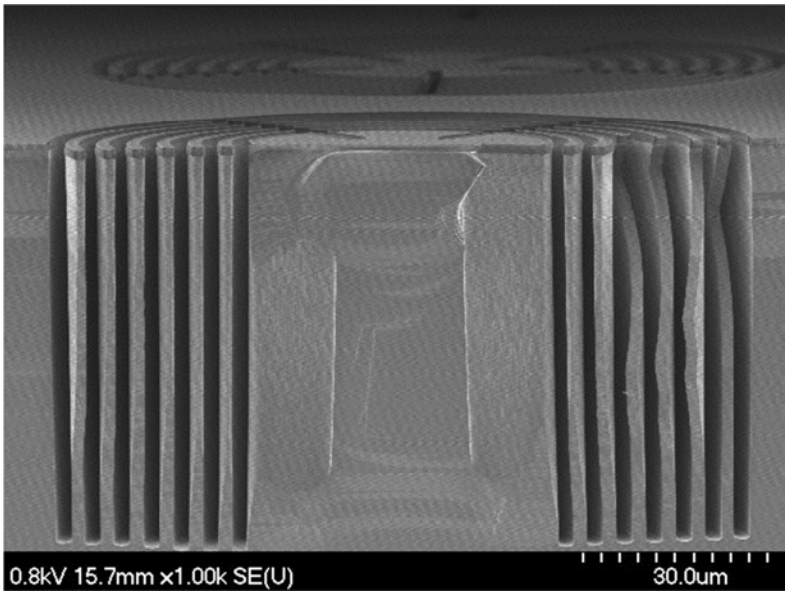


Figure 9: Cross-section through a trench capacitor after DRIE (Step 1). The TSV that normally exists along the central axis of each trench capacitor is not shown in this picture.

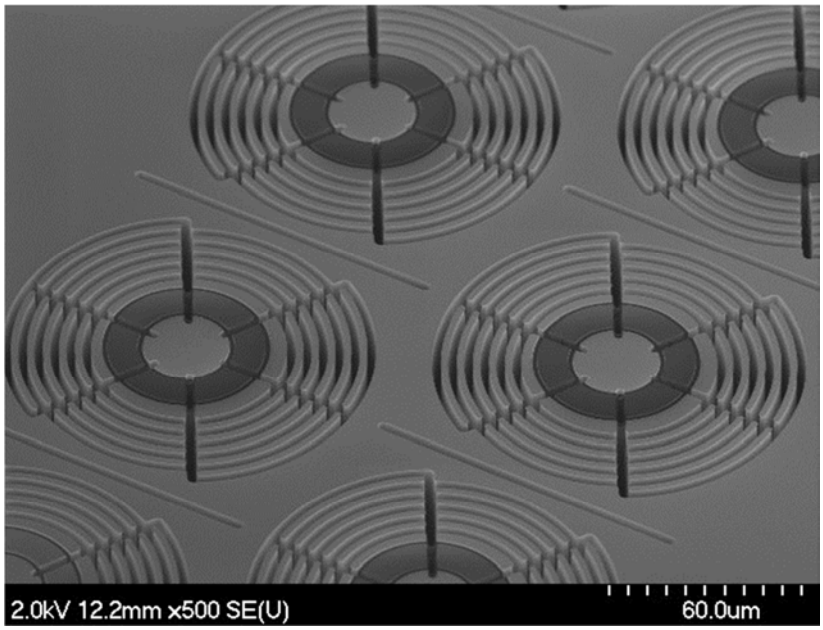


Figure 10: Surface SEM of TSV and trench-capacitors after the trench capacitor etch (Step 1).

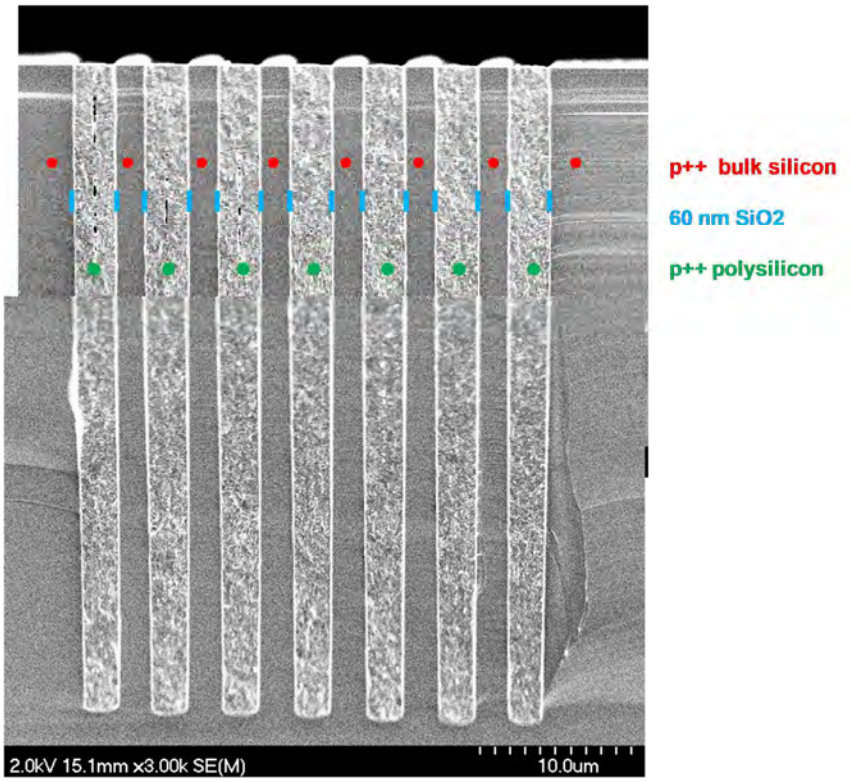


Figure 11: Composite SEM of the trench capacitor after poly fill and CMP. (Step 4)

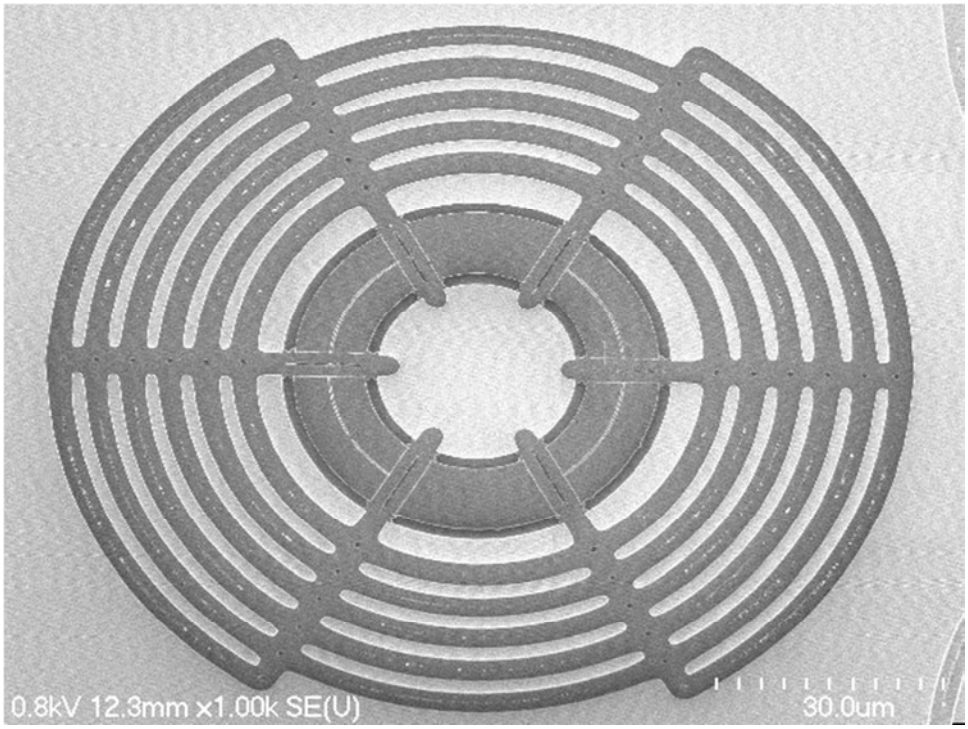


Figure 12: Surface SEM images of a TSV and trench capacitor after poly fill and CMP (Step 4).

There are 3 design splits and 2 process options for forming the trench capacitors. The 3 design splits are shown in Figure 13. The process options involve growing either 600 angstroms or 900 angstroms of thermal oxide on the capacitor side-walls. If a 900 angstrom thermal oxide is grown, the 3 design splits give capacitances of 72, 92, and 116 pF. If a 600 angstrom thermal oxide is grown, the 3 splits give capacitances of 105, 130, and 163 pF. Experimental test results for the capacitors are shown in Figure 14.

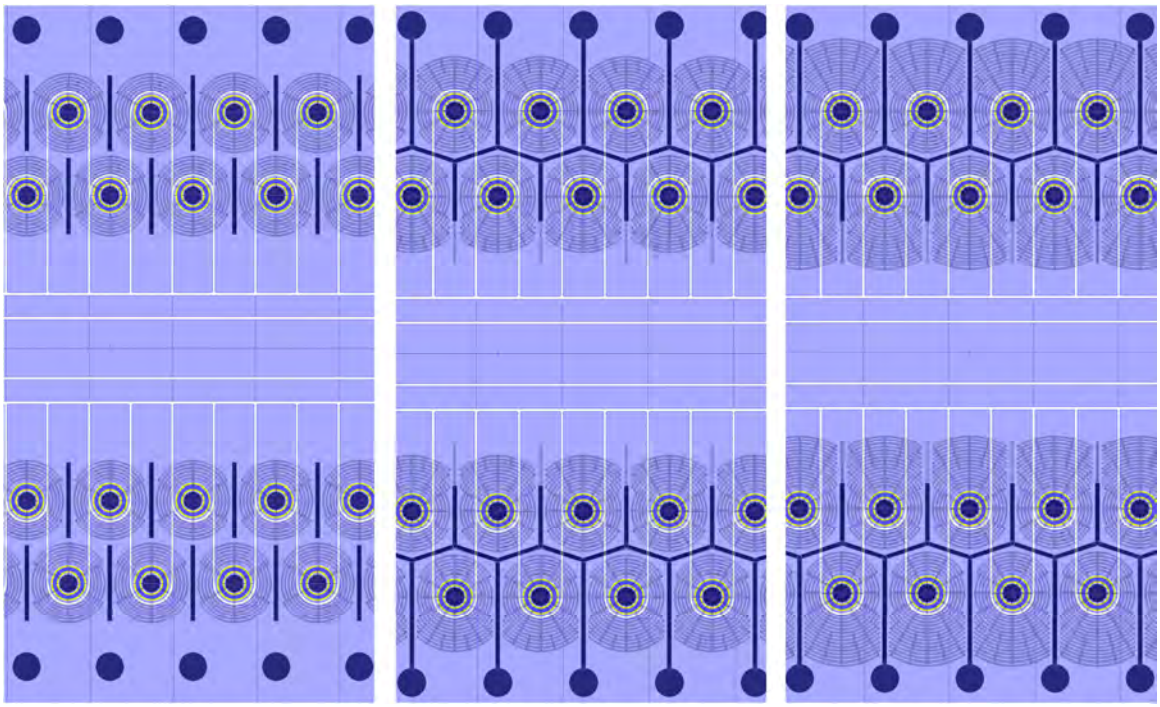


Figure 13: 3-layout plot of the 3 capacitor designs

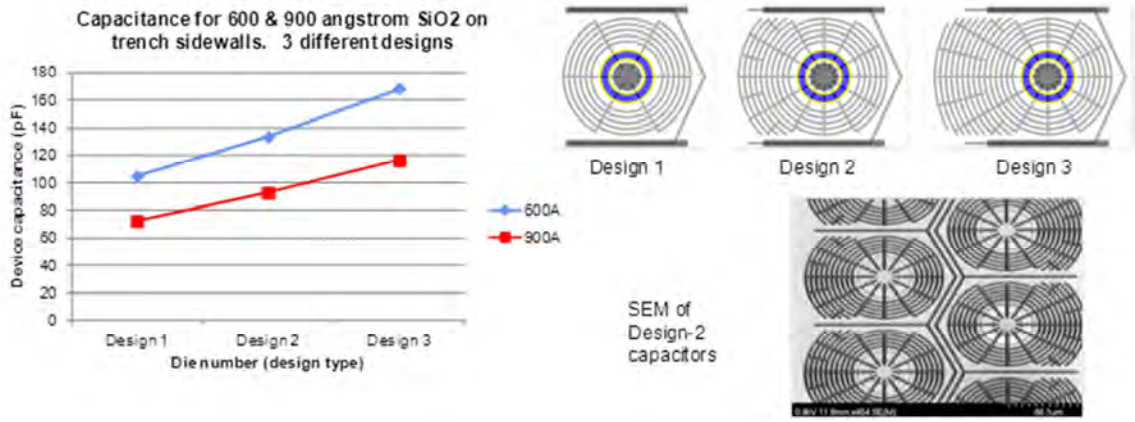


Figure 14: Capacitor test data and designs.

The across-the-wafer uniformity of trench capacitor properties was typically within a few percent. Figure 15 shows results from one particular wafer, processed with 900 angstroms of trench-capacitor oxide that yielded:

8 die with Design #1, with an average capacitance of 72.0 pF;
10 die with Design #2, with an average capacitance of 92.5 pF; and
11 die with Design #3, with an average capacitance of 116 pF.

The breakdown voltages on all of the capacitors, regardless of the sidewall oxide thickness, were typically greater than 18 volts.

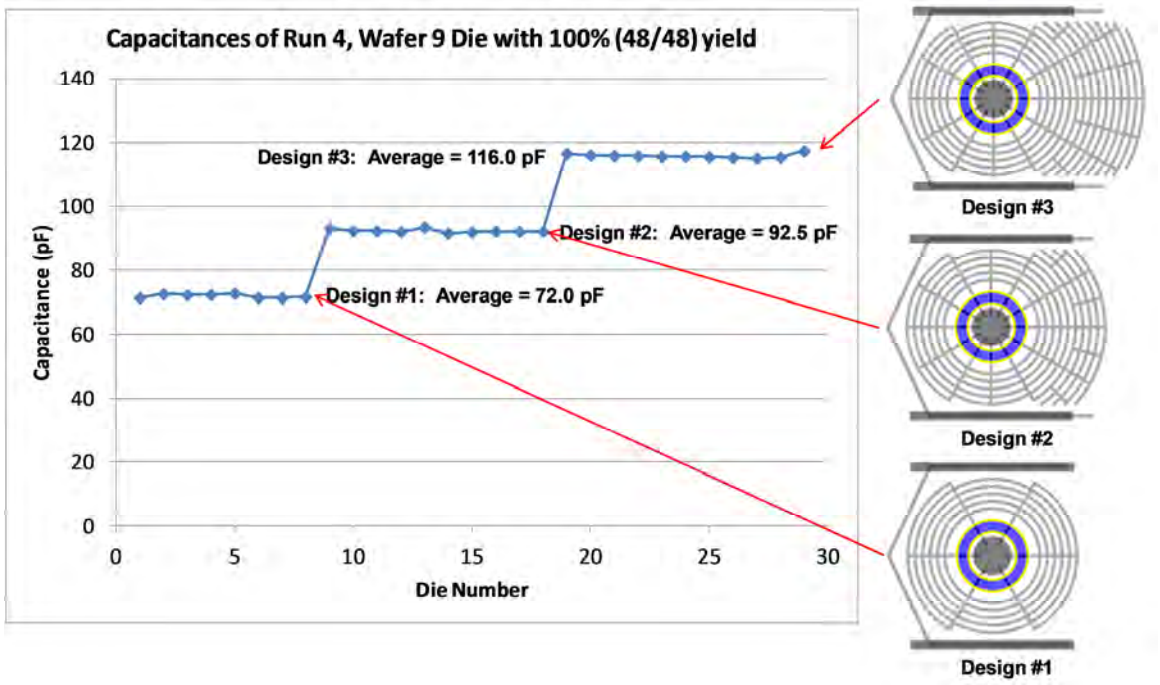


Figure 15: Trench capacitor test results from Run #4, Wafer #9.

The intra-die uniformity of trench capacitor values was also typically within a few percent. Figure 16 is a layout plot showing and labeling all 48 trench capacitors. There are 24 capacitors on the left-hand side and 24 capacitors on the right-hand side of each die. Figure 17 shows the measured capacitance values on an unpackaged die. It is interesting to note from Figure 17 that differences in the lengths of the DC electrodes are measureable (the odd-numbered electrodes are 120 µm longer than the even-numbered ones). Differences in the widths are also measurable (electrodes 2, 3, and 4 are all 100 µm wide; 5-22 are 60 µm wide); as are overall area effects (electrode 1 is 684 x 140 µm; electrode #23 is 513 x 260 µm; and electrode #24 is connected to the DC rail which is 3000 x 100 µm—the DC rails are patterned in 3rd metal).

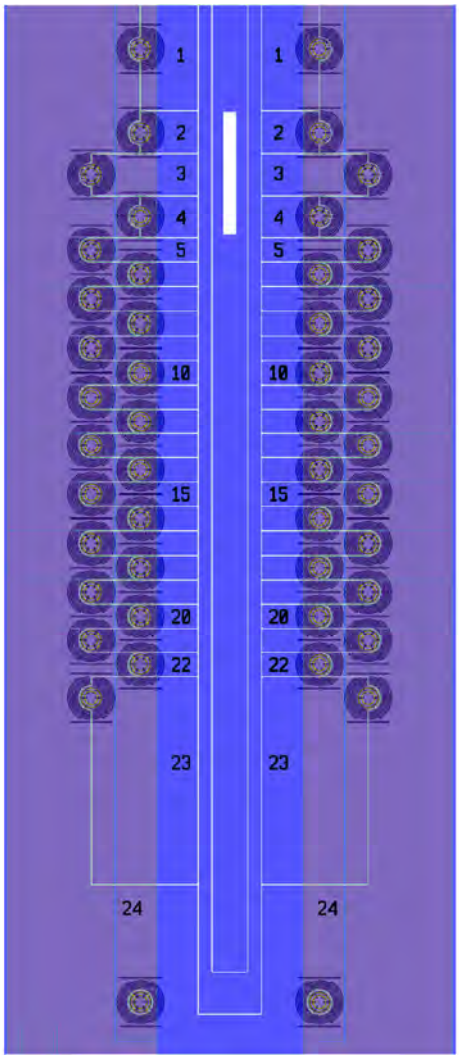


Figure 16: Layout plot identifying the various capacitors by Row number. The design of the die has perfect left-right symmetry: capacitors on the left in any given row are designed to have the same capacitance values as their counterpart on the right.

When the trap die are bonded to the interposer and packaged, the interposer leads add an additional ~5-15 pF to the capacitance, depending on the length and width of the interconnects on the interposer.

Capacitor breakdown voltage is determined by ramping the voltage across a capacitor from 0 to 40 volts, and measuring the leakage current as a function of voltage. When breakdown occurs, the leakage current spikes to the compliance limit of the tester (set at 1E-3 amps). Breakdown is a destructive event. Once breakdown occurs the capacitor is permanently damaged.

The breakdown voltages of 100 individual capacitors from four different locations on a wafer were measured. Figure 18 shows the breakdown data from each of the 100 individual capacitors.

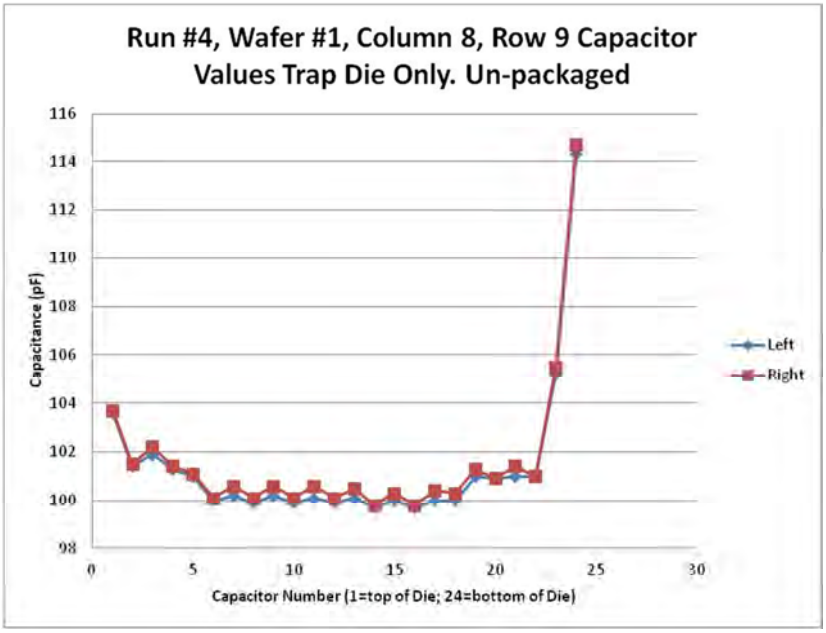


Figure 17: Measured capacitances of the DC electrodes.

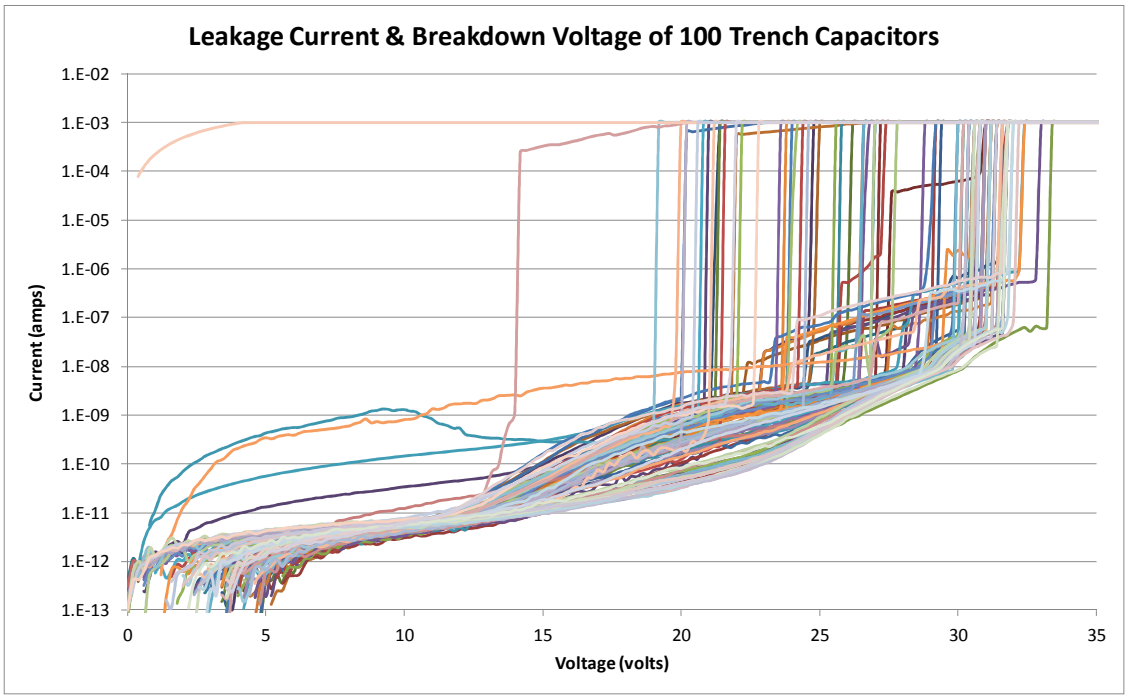


Figure 18: Leakage current and breakdown voltage of 100 trench capacitors.

3.) Making Ohmic Contacts:

Once the TSVs and trench capacitors have been formed, an additional CVD (Chemical Vapor Deposition) SiO2 layer of up to 1 µm is deposited. The SiO2 is patterned with photoresist, the photoresist is thermally reflowed to induce a slope, and the wafer is etched using a RIE (Reactive Ion Etch) process that transfers the slope from the photoresist into the SiO2. Once the underlying silicon layer has been reached, a platinum silicide layer is formed. Figure 19 is a SEM of a portion of a trap after silicidation. The inner-most parts of trench capacitor spokes are silicided, as are the tops of the TSV cores. The first metal in the contacts forms a short between each TSV and its associated trench capacitor. Elsewhere on the trap die, ground connections are made to the bulk silicon wafer (larger round circles) and to trenches that help to isolate one DC region from its neighbors (long narrow bars).

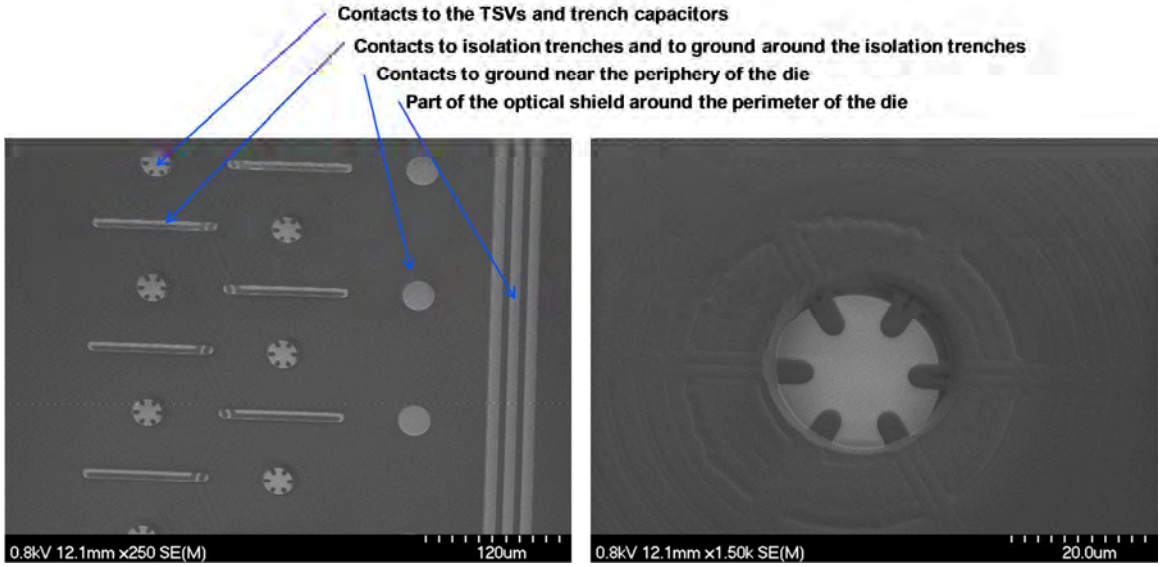


Figure 19: SEM images after contact silicidation. Low magnification (left) and higher magnification (right).

4.) Patterning 3 layers of front-side metal:

The metallization process through 1st metal and 1st dielectric is routine. 1st metal is a 1.5 µm-thick layer of gold surrounded below by a TiW/Pt adhesion/diffusion barrier, and above by a Ti adhesion layer. As shown in the layout plot in Figure 20, 1st metal (M1) is a large ground plane, interrupted only where there are TSVs. At the locations of the TSVs, 1st metal is patterned into 50 µm-diameter circles that are separated from the ground plane by 5 µm gaps. The 50 µm-diameter circles are connected to the TSVs below through sloped contacts and to the 2nd metal above by sloped vias. The dielectric between the TSVs and 1st metal is 1.5 µm thick; the dielectric between 1st metal and 2nd metal is 10 µm thick. Vias in the second dielectric are also formed by thermally sloping photoresist and etching the vias in a recipe that transfers the slope into the SiO2.

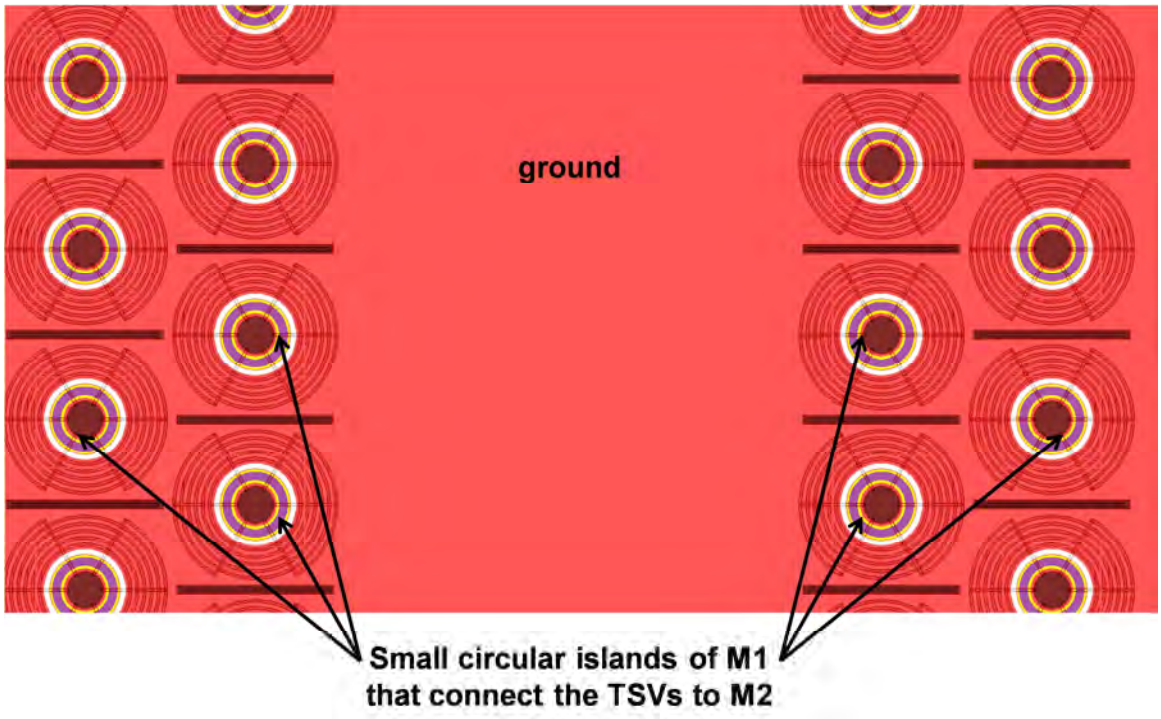


Figure 20: Layout plot showing 1st metal (red), the trench capacitors (gray) and the TSVs (blue circles surrounded by yellow). 1st metal is a large ground plane, interrupted above the TSVs to form small islands that connect the TSVs below to 2nd metal above.

Second metal is 1.5 µm of gold with 300 angstroms of Ti above and below to ensure good adhesion of the gold to the SiO2 dielectric. Figure 21 and Figure 22 show some of the design options for 2nd metal. The topography associated with the vias down to 1st metal is clearly evident in these SEM images.

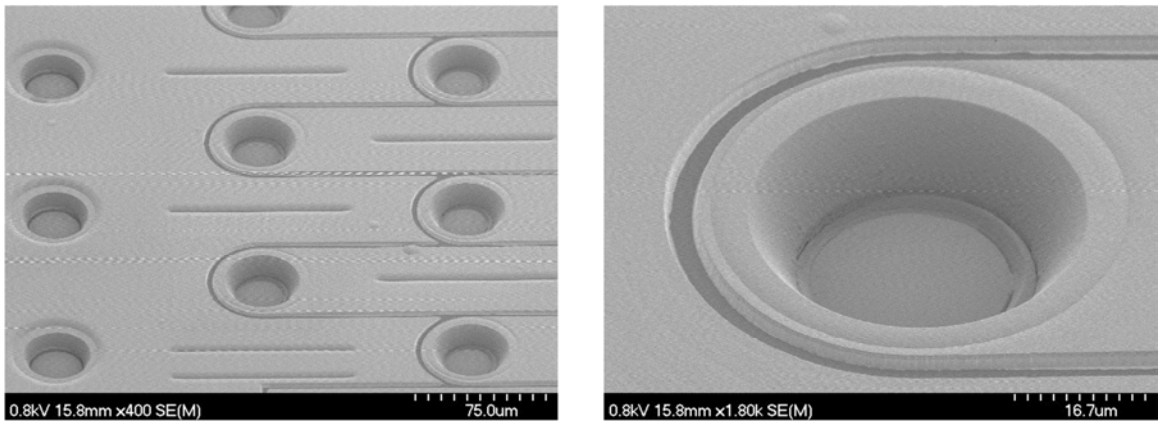


Figure 21: SEM images of a wafer after etching sloped vias and patterning 2nd metal: Portion of a trap (left) and individual via (right).

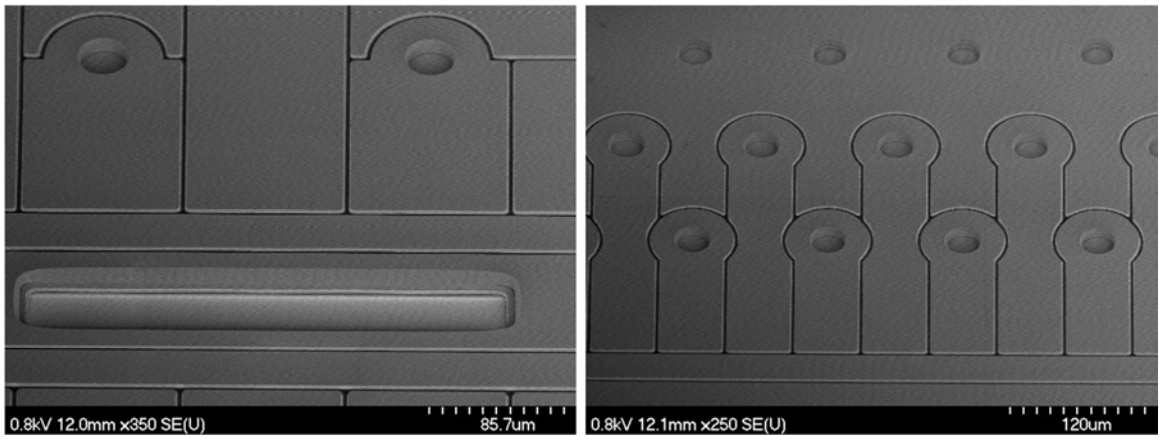


Figure 22: SEM images 2nd metal. Design Option #2.

After 2nd metal has been patterned, 13 µm of CVD SiO2 is deposited over the entire wafer, and a CMP operation is performed to remove most of the topography associated with 2nd metal and 1st to 2nd vias. Figure 23 shows portions of the trap wafer after this CMP operation has been performed. After CMP an additional layer of 3.5 µm of TEOS SiO2 is deposited. This 3.5 µm SiO2 is the permanent dielectric between 2nd and 3rd metal.

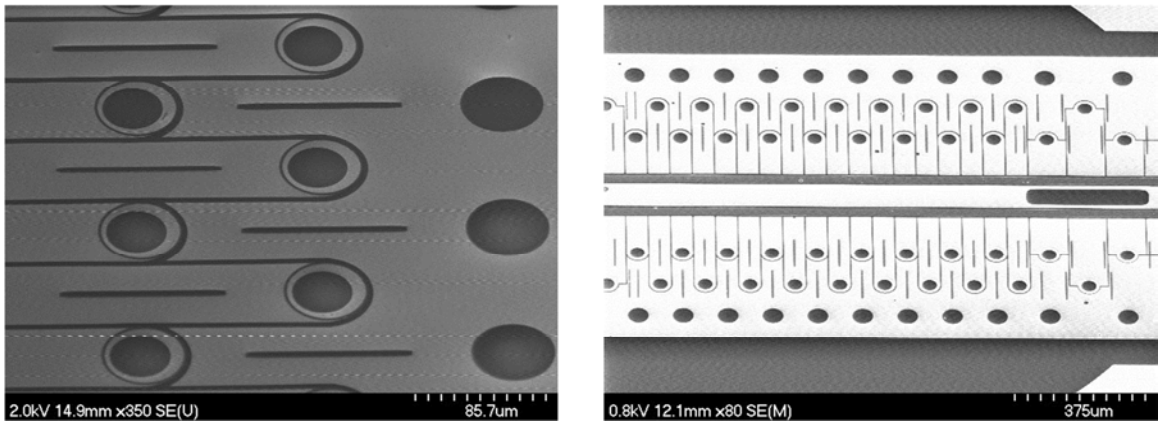


Figure 23: SEM images of a wafer after depositing 14 µm SiO2 and doing CMP to planarize the vias: Portion of a trap (left) and entire trap die (right).

Via plug: A via is etched through the 3.5 µm SiO2 prior to 3rd metal deposition. Optionally, a via plug (also 3.5 µm thick) is used to fill the via and thereby improve the planarity of the 3rd metal surface. Figure 24 shows optical photographs of a trap die after the via plug has been deposited (left), and after 3rd metal has been patterned and deposited (right). As is evident in the right-hand side of Figure 24, there is very little print-through into 3rd metal of anything other than the via plugs. The various colors on top of the metal layers are due to the TiW and SiO2 layers that still cover all of the gold.

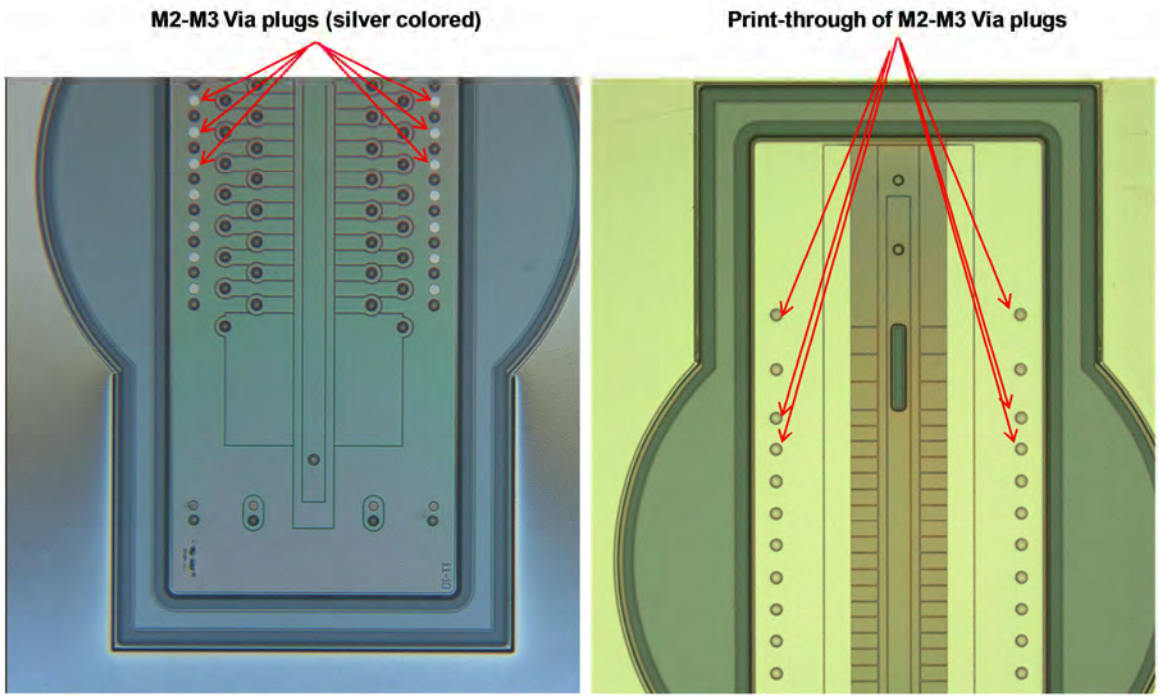


Figure 24: Run #3 after 2nd-via plug lift-off (left), and after 3rd metal (right).

Figure 25 and Figure 26 show SEM images of the trap die after 3rd metal has been patterned and all of the SiO2 above the 1st, 2nd, and 3rd layers of gold has been etched away.

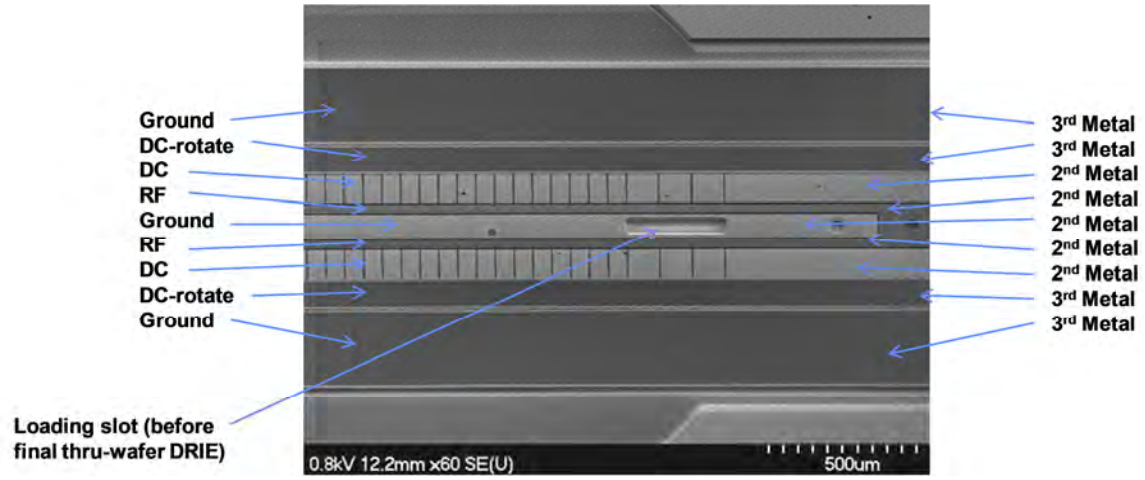


Figure 25: SEM of Run 3 after front-side SiO2 removal.

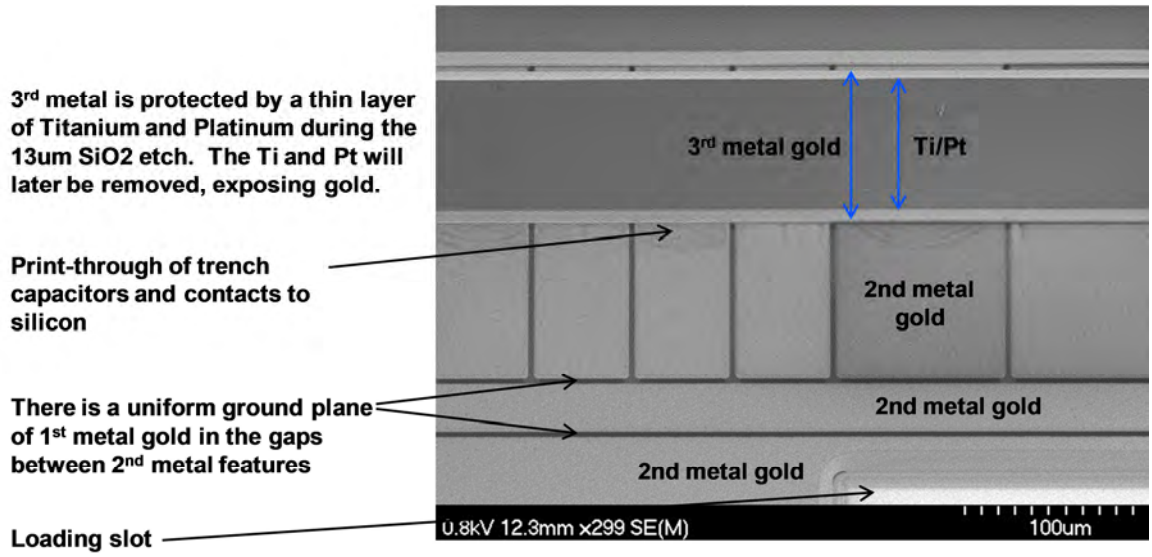


Figure 26: SEM after 3rd metal showing some of the surface topography.

After all 3 metal layers have been patterned, the wafer is subjected to a very long (>2 hour) RIE step that anisotropically removes all exposed SiO2, leaving only gold. An anisotropic etch removes oxide vertically, but not laterally. The RIE recipe has near-infinite selectivity to metal, so the gold is barely touched. Optionally the wafer is then subjected to a ~3 µm BOE (Buffered Oxide Etch) process that etches the SiO2 laterally, leaving overhanging metal features. Figure 27 shows a portion of a trap die after the BOE etch.

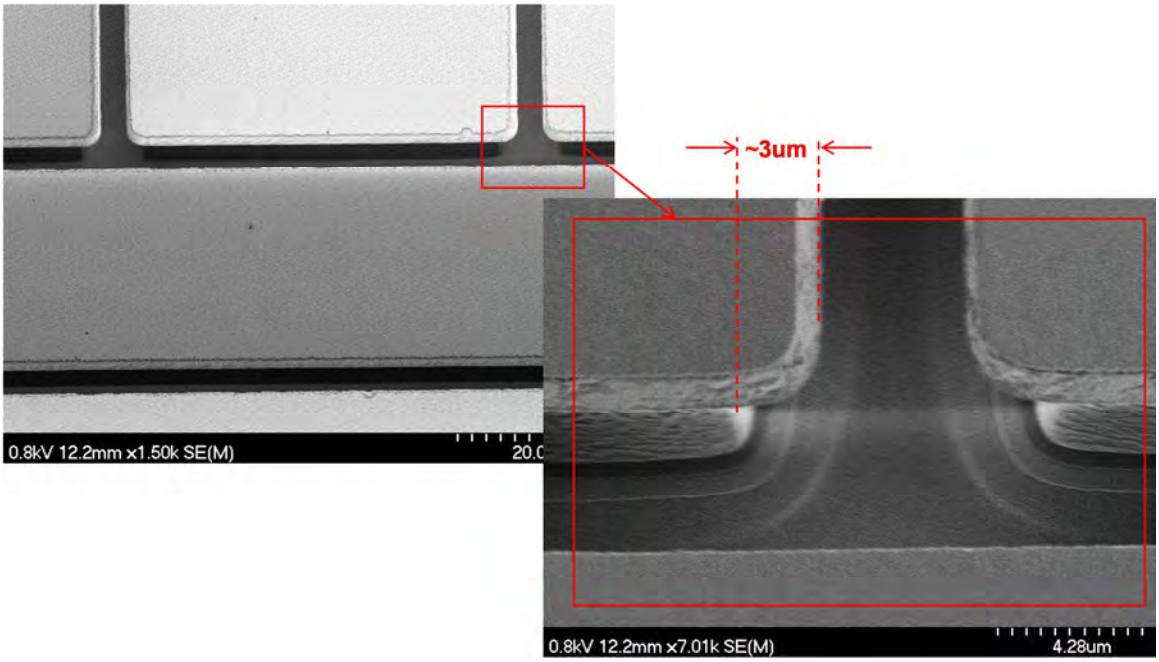


Figure 27: Second metal on a trap after a BOE etch.

After all metal patterning is complete, the wafer is flipped over and back-side processing is performed.

5.) Patterning Back-side Metal

Figure 28 shows the back-side of a BGA trap die after back-side metal has been patterned but before the loading slots have been etched. The two main features evident in Figure 28 are the silicided contacts, and the patterned back-side metal. Forty-eight (48) of the silicided contacts make electrical contact to the cores of the 48 TSVs; another 28 silicided contacts are used to make ground connections to the bulk silicon part of the die. Figure 29 is a close-up of the back-side of the die, showing more clearly where the TSVs and bond pads are located.

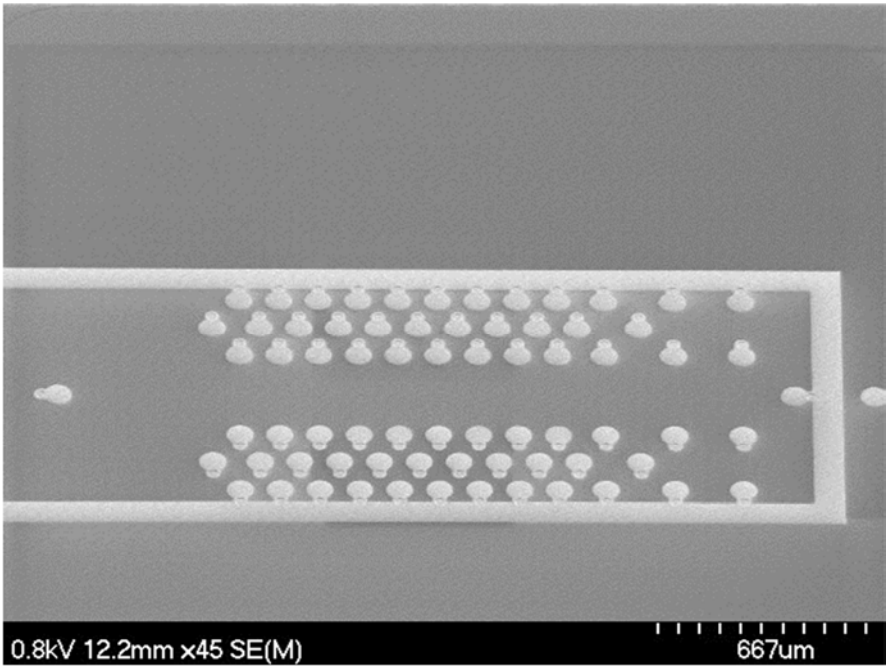


Figure 28: Back side of a BGA die.

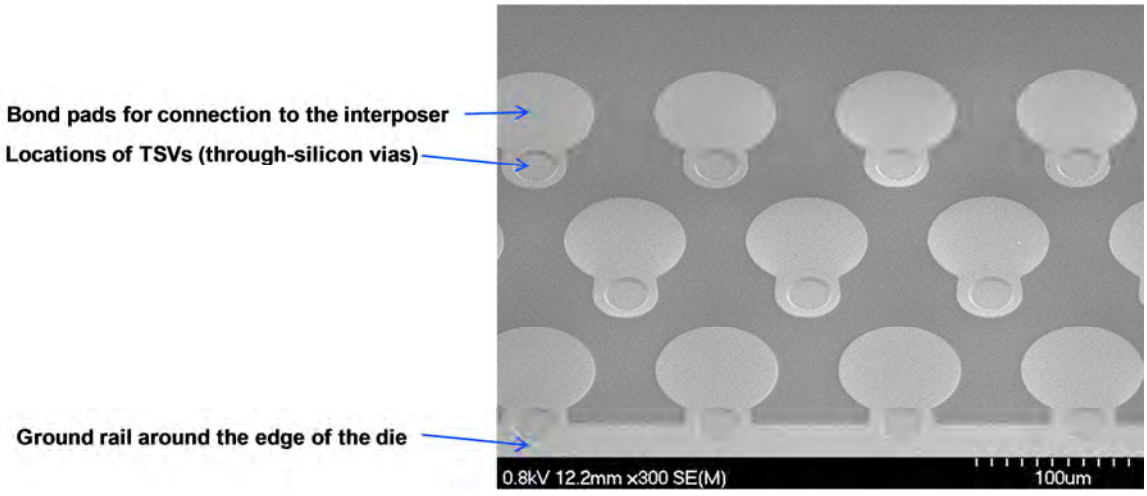


Figure 29: Close-up of the back-side of a BGA die.

6.) Making Loading Slots:

Slots in the trap die allow passage of a thermal flux of neutral atoms for ion loading. Two separate DRIE masks are used to pattern the loading slots: one mask is used to etch the front-side of the wafer, and the other is used to etch the back-side. The photomasks that define the loading slots also open up the perimeters of each die so that after the loading-slot DRIE etch step is complete, the die are singulated (separated from one another and from the bulk wafer on which they were formed). Figure 30 is a SEM showing a portion of a trap wafer after the final front-side loading-slot etch. The parts identified by the red arrows (the loading slot and the die singulation features) are etched away; the parts identified by the green arrows (the trap die and the handle portion of the wafer) are not etched. The Die singulation features are extra wide near the center of the trap die so that tweezers can be used to pull the trap die off of the carrier wafer.

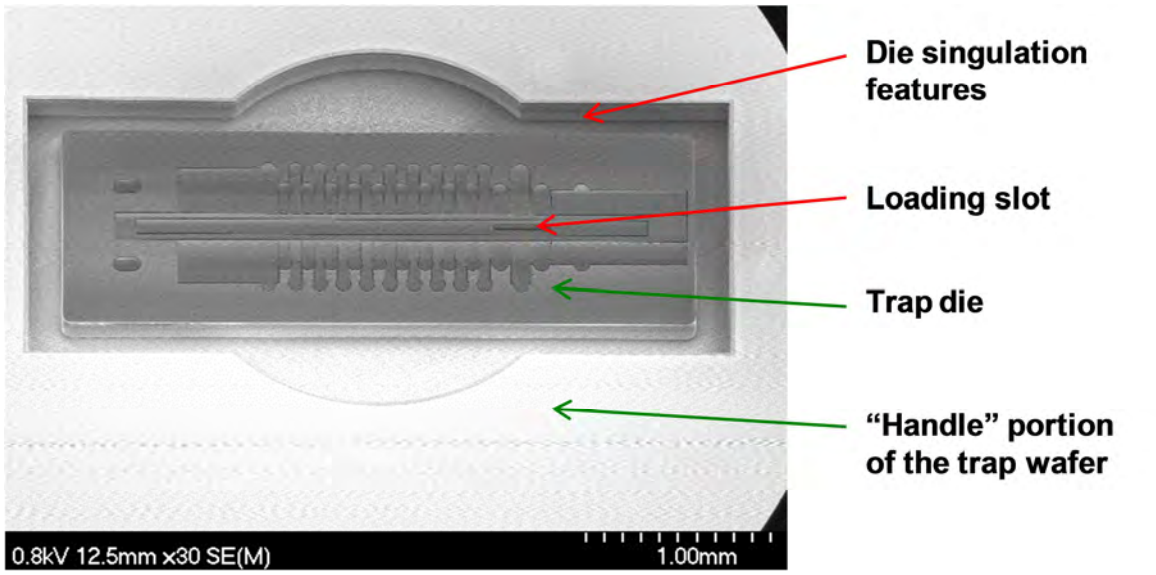


Figure 30: SEM of a released trap die, still attached to a carrier wafer, and still surrounded by the non-die "handle-portion" of the trap wafer.

Figure 31 shows a trap die after it has been removed from its carrier wafer. It is now ready to be bonded to an interposer.

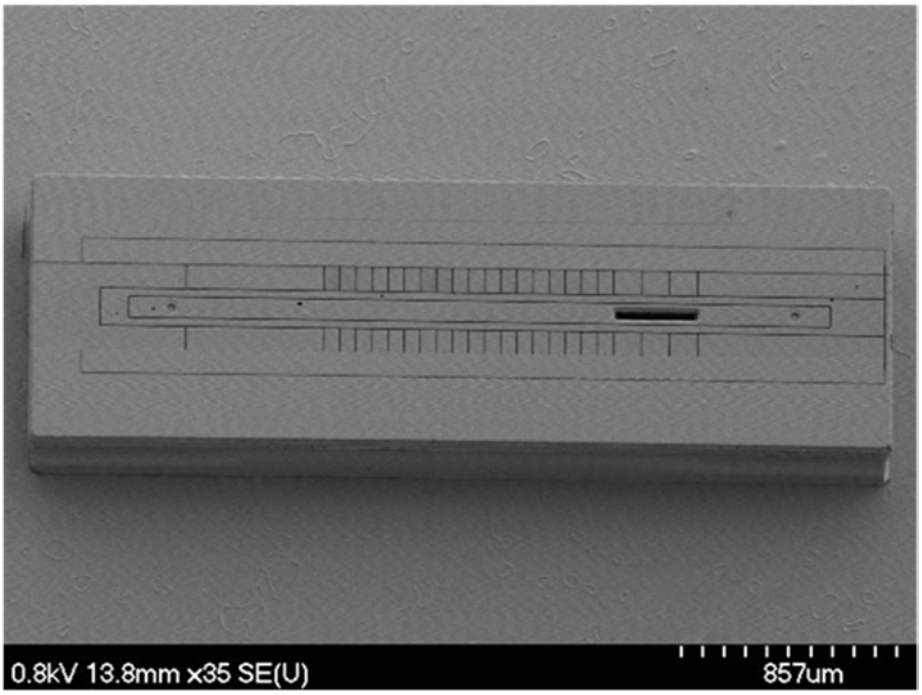


Figure 31: Trap die ready to be bonded to an interposer.

Figure 32 shows the back-side of a trap die. The back-side loading slot is oversized relative to the front-side loading slot so as to allow a greater flux of atoms from the oven to reach the front side of the trap die. The entire loading slot is coated with gold to minimize charge build-up.

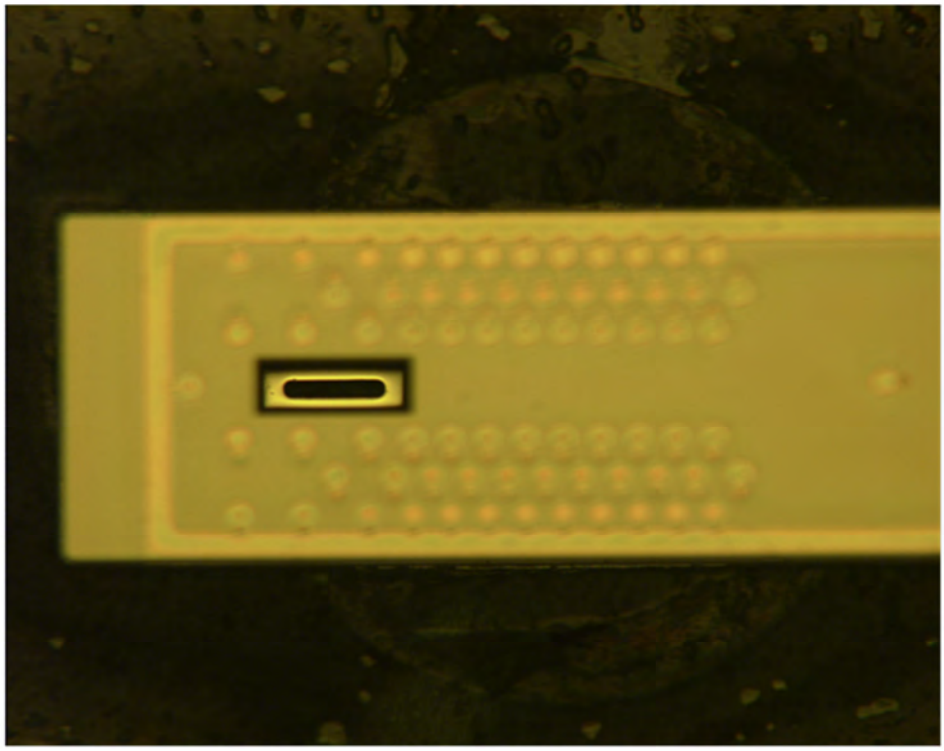


Figure 32: Back-side of a trap die, focused on the shelf part-way through the loading slot.

2.2.2 Interposer Processing

The interposer is a separate die (separate from the trap die) whose purposes are: 1.) to elevate the trap die above the rim of the package; and 2.) to carry the electrical signals from the package to the trap die. The process for making the interposer involves 9 separate masks steps, as summarized below:

1.) *1st metal.* The main purpose of 1st metal is to form a uniform ground plane beneath all of the signal-carrying lines. 1st metal is 1.7 μm of Au, with Ti and Pt adhesion/barrier layers above and below it. After 1st metal has been patterned, a blanket layer of 4 μm of SiO2 is deposited.
2.) *2nd metal.* 2nd metal (also 1.7 μm of Au surrounded above and below by Ti and Pt) carries electrical signals horizontally to the trap region from the middle of the interposer. After 2nd metal has been patterned a blanket layer of 6 μm of SiO2 is deposited.
3.) *1st via.* The first via process etches holes through the SiO2 dielectric down to the metal layer beneath. In cases where there is a 2nd metal feature under the via, the etch stops on 2nd metal. In other cases where there is no 2nd metal feature beneath the via, the etch continues down to 1st metal (ground). There are no locations on the die where there is neither a 1st metal nor a 2nd metal feature.
4.) *3rd metal.* 3rd metal (1.7 μm Au) carries electrical signals in from the edges of the interposer to 2nd metal. After 3rd metal has been patterned a blanket layer of 3 μm of SiO2 is deposited.
5.) *2nd via:* 2nd via opens up holes though the 3 μm of SiO2 down to 3rd metal. Holes near the perimeter of the interposer expose 3rd metal pads for wire-bonding to the package. Holes near the center of the interposer expose 3rd metal pads for solder-bonding up to the trap die.
6.) *4th metal.* 4th metal (1.7 μm Au) is essentially a ground plane but also has features (metal pads) at the locations of 2nd vias. These extra metal pads at the 2nd via openings create larger areas for the solder connections to the trap die.
7.) *Bond pads.* Optionally, an additional layer of metal is deposited. Its thickness and properties are optimized either for solder bonding or wire bonding.
8.) *Front-side loading slots.* Holes for the ion loading slots are DRIE-etched ~300-350 μm into the front-side of the wafer
9.) *Back-side loading slots.* Holes for the ion loading slots are DRIE-etched ~1000 μm in from the back-side of the wafer. The front-side loading slot holes and the back-side loading slot holes meet 300 μm from the front surface of the interposer, creating a continuous opening from back-to-front.

The individual interposer die are singulated by dicing the interposer wafer.

Figure 33 shows an optical photograph of the central portion of an interposer after 3rd metal has been patterned. Figure 34 and Figure 35 show SEM images of the interposer after 2nd via. Figure 36 is a SEM after all processing on the interposer wafer is complete and the wafer is ready for dicing. The atom loading slot is clearly evident in Figure 36.

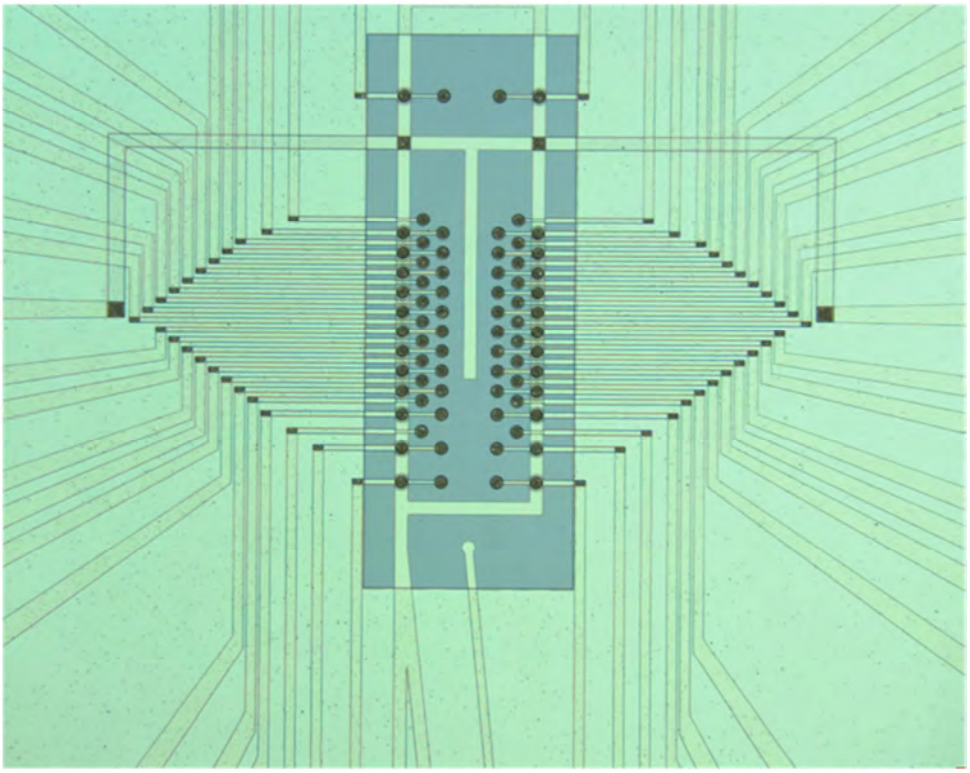


Figure 33: Optical photograph of the interposer wafer after 3rd metal patterning.

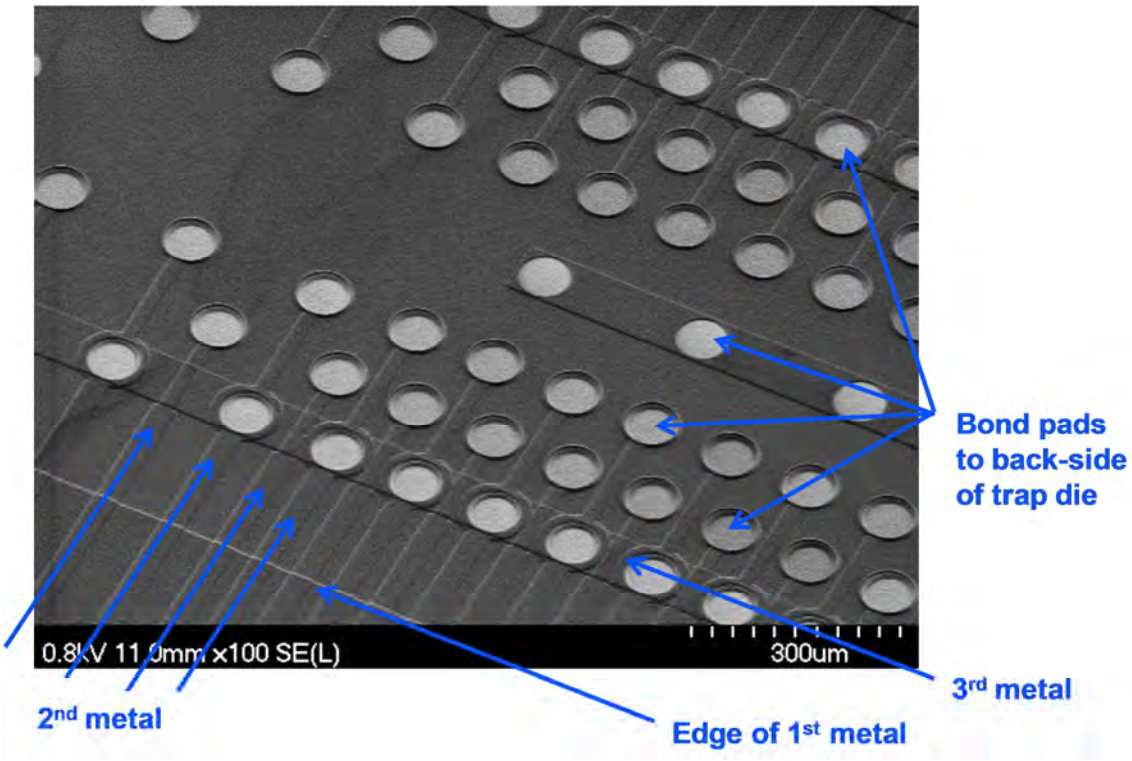


Figure 34: SEM of the interposer after 2nd via etch.

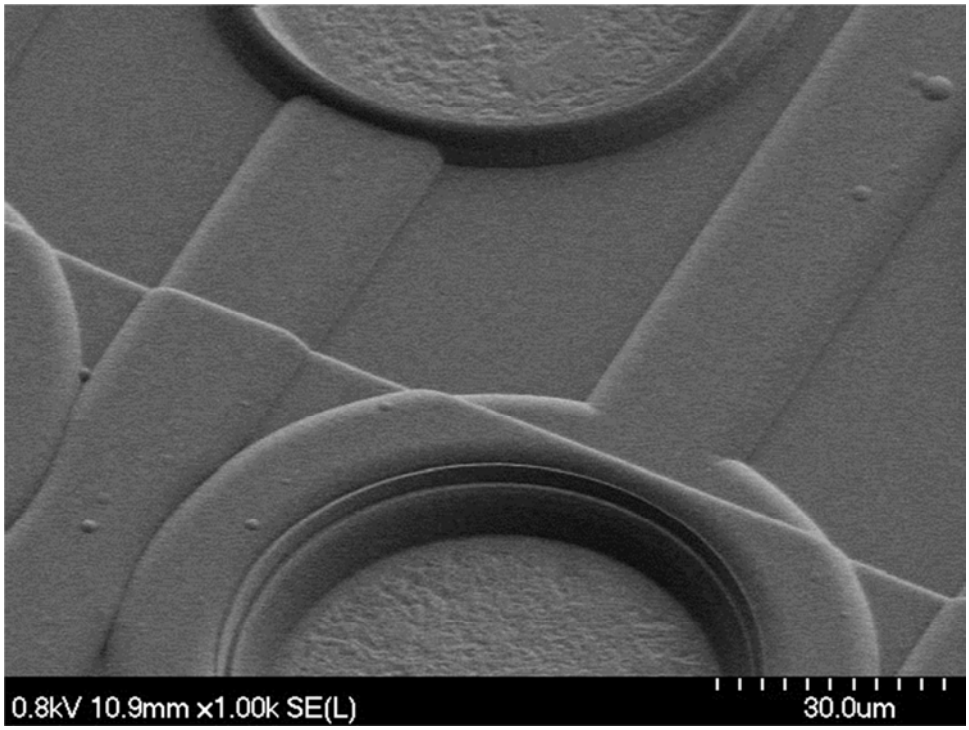


Figure 35: Close-up via where 2nd metal steps down to 1st metal. The total oxide thickness separating 3rd metal from 1st metal = 10 μm.

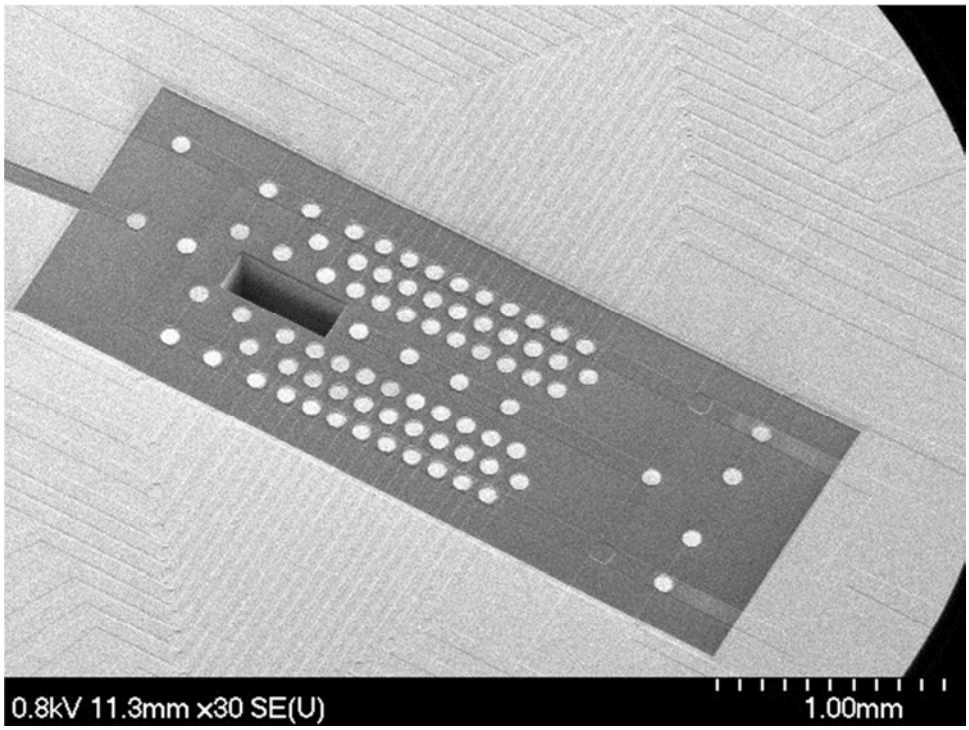


Figure 36: SEM of the interposer after 4th metal has been patterned and deposited. The 4th metal features include bond pads and an outer ground plane.

2.2.3 Assembly

The term "assembly" refers to the sequence of steps involved in taking a separate trap die, an interposer die, and a CPGA package, and bonding them together into a single unit. The steps in the assembly sequence are:

1.) Attaching gold studs to the bond pads on top of the interposer.
    a. Optionally, putting gold and tin on the bond pads on the bottom of the trap die.
2.) Attaching the trap die to the interposer using the gold studs as interconnects.
    a. If gold and tin are put on the bottom of the trap die, using a solder-reflow process to attach the traps to the interposers
    b. If no additional gold and tin are used on the trap die, using ultra-sonic bonding to attach the traps to the interposers.
3.) Putting a separate layer of gold studs directly on the base of the CPGA package
4.) Attaching the interposer (which now contains a trap die) to the CPGA package using an ultra-sonic bonder.
5.) Attaching wire bonds.
    a. ...from the package to the interposer. There are 48 bond wires for the DC signals, and an additional 51 wires for ground.
    b. ...from the package directly to the trap die. There is one wire bond for the RF signal that goes directly from the package to a 3rd metal feature on the trap die that carries the RF signal.

Figure 37 shows the tool used to attach gold studs. It is a conventional wire bonder, programmed to leave very short bond wires (only ~75 µm from base to tip). Figure 38 and Figure 39 are an optical photo and a SEM of an interposer after gold studs have been attached. Figure 40 shows wire bonds attached from the interposer down to corresponding bond pads on the package.

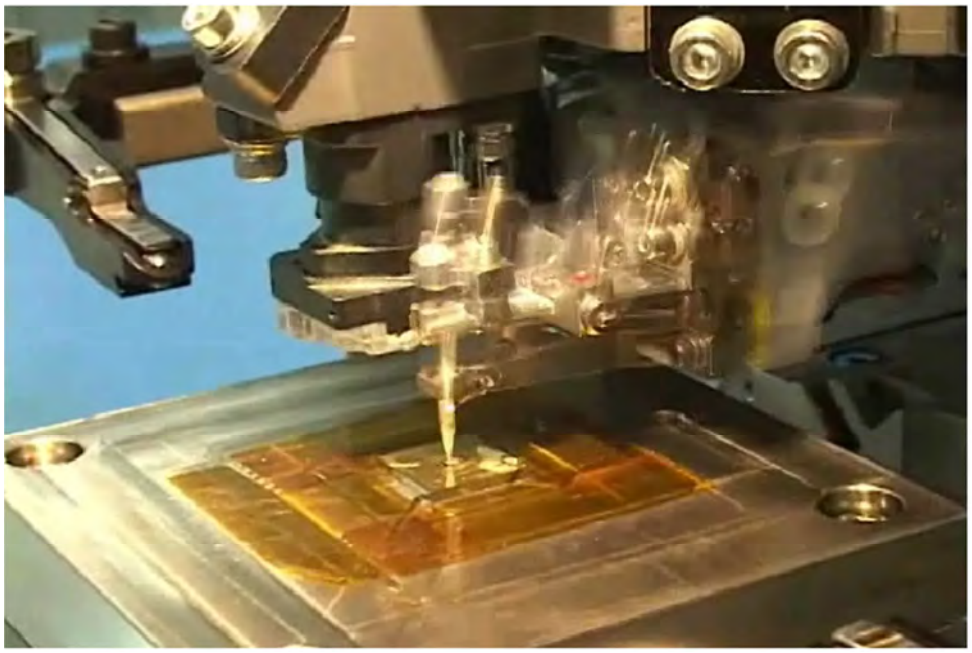


Figure 37: Wire bonder being used to attach gold studs to the interposer.

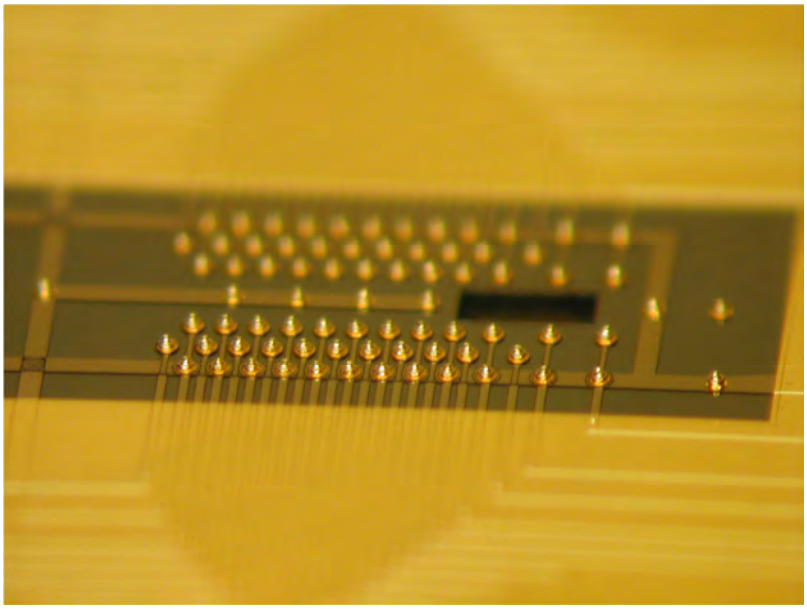


Figure 38: Optical photo of gold studs attached to the interposer.

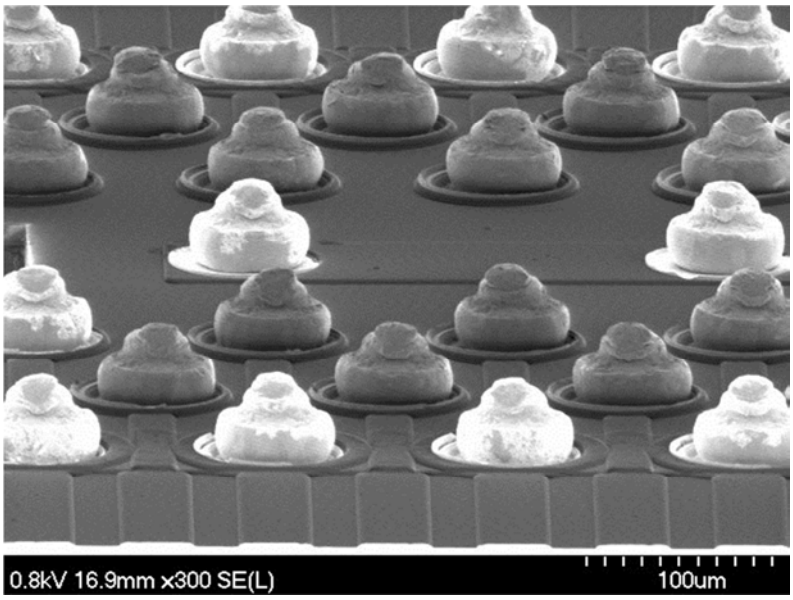


Figure 39: SEM of gold studs attached to the interposer. The studs that are attached to ground appear to glow more brightly than those connected to the leads to the DC electrodes.

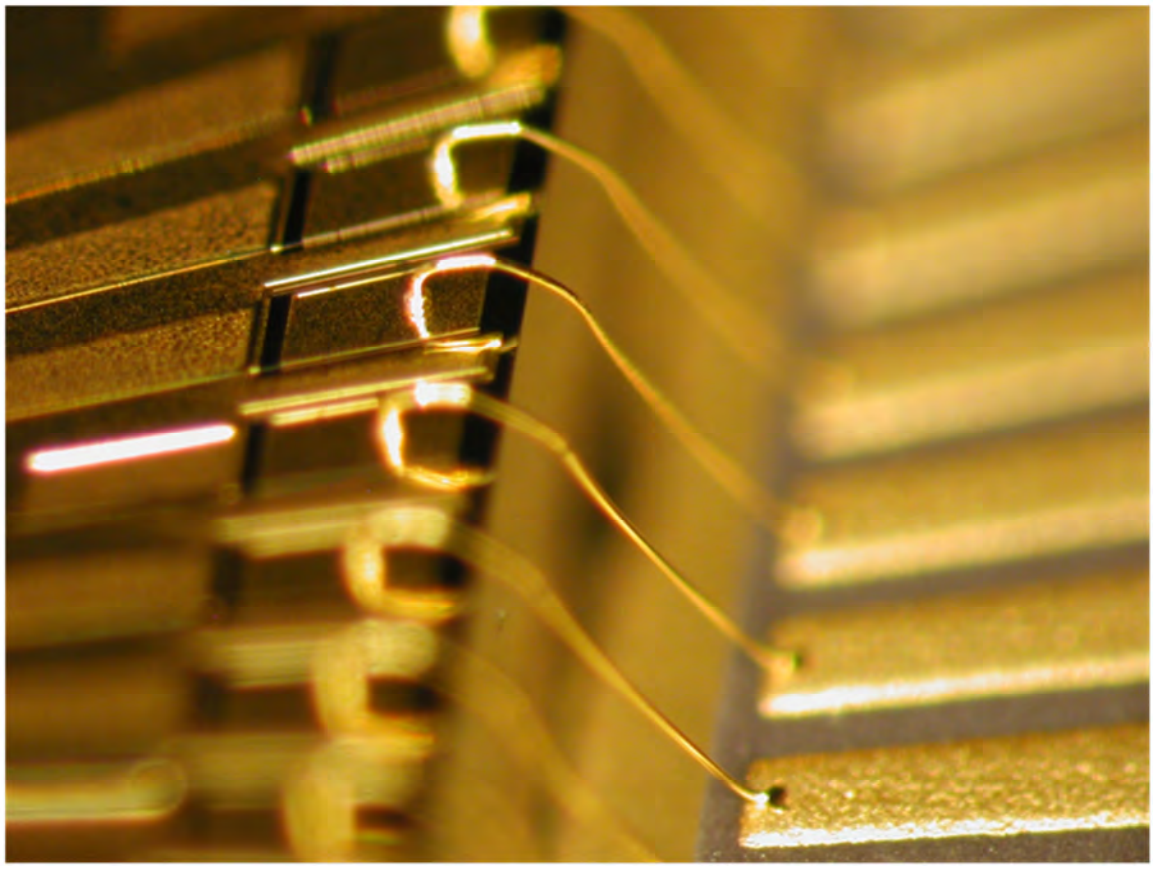


Figure 40: Wire bonds from the interposer to the package.

2.3 Deliverables

A total of 3 fully-assembled, fully-functional trap assemblies were delivered to GTRI under the BGA contract. Several test parts with one or more defects were also delivered.

The three deliverable traps were all shipped on May 27th, 2014. All three trap die were from Run #4, Wafer #1. They were:

1. **BGA Die #11-09.** Capacitor values on the pre-packaged die were 130.2 +/- 2.7 pF.
2. **BGA Die #08-09.** Capacitor values on the pre-packaged die were 101.0 +/- 3.0 pF.
3. **BGA Die #15-09.** Capacitor values on the pre-packaged die were 163.7 +/- 2.6 pF.

Figure 41 through Figure 43 show the properties and yields of the capacitors from those 3 trap assemblies before being assembled with interposers. Figure 44 shows how the interposer changes the capacitance of the overall trap assembly. Figure 45 and Figure 46 are optical photos of two of the traps.

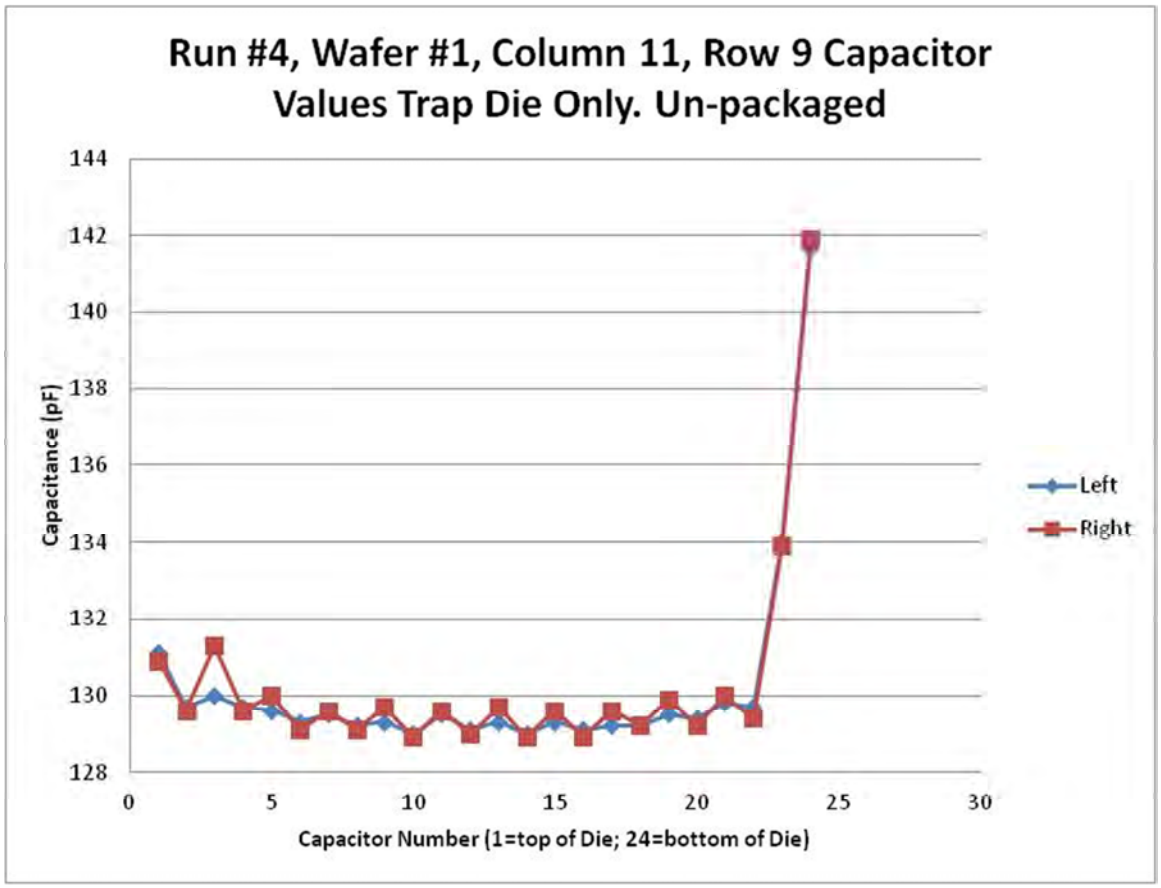


Figure 41: Measured capacitances of the DC electrodes on Die 11-09. Yield: 48/48 = 100%

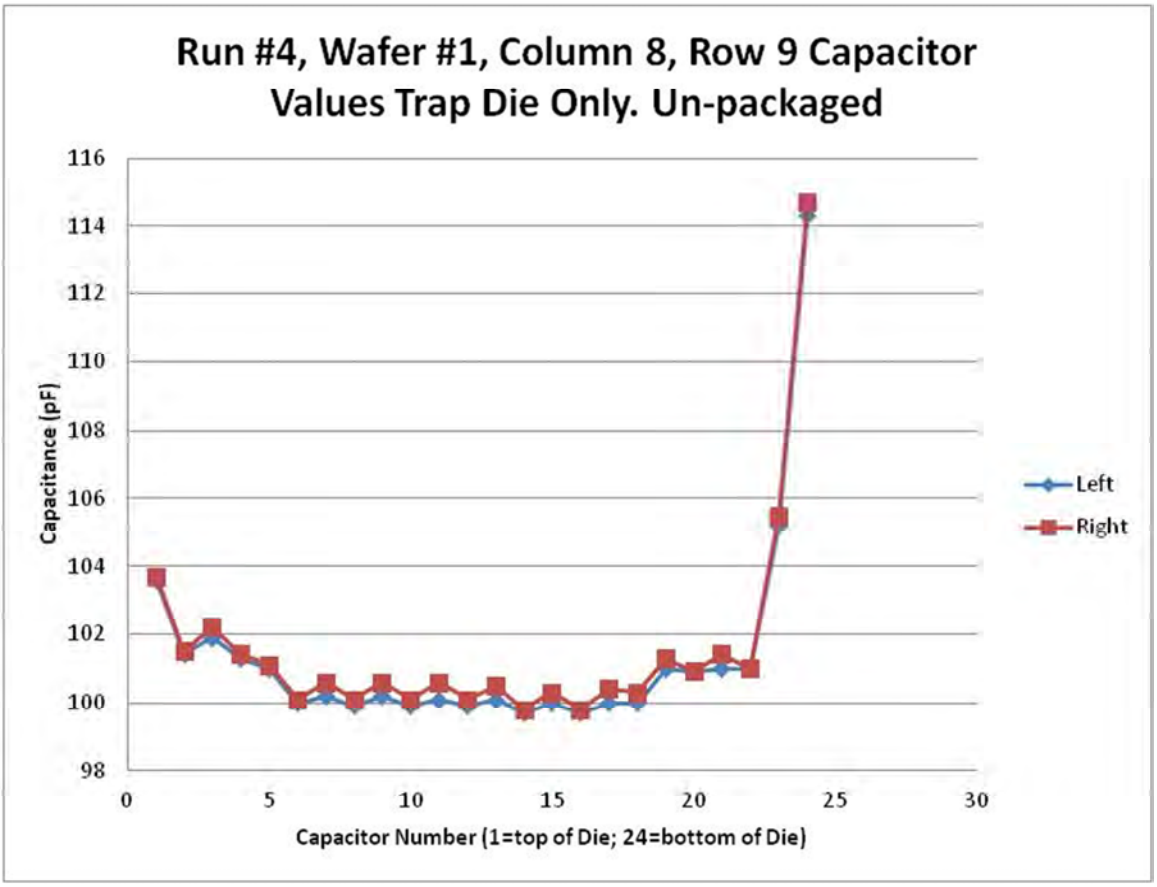


Figure 42: Measured capacitances of the DC electrodes on Die 08-09. Yield: 48/48 = 100%

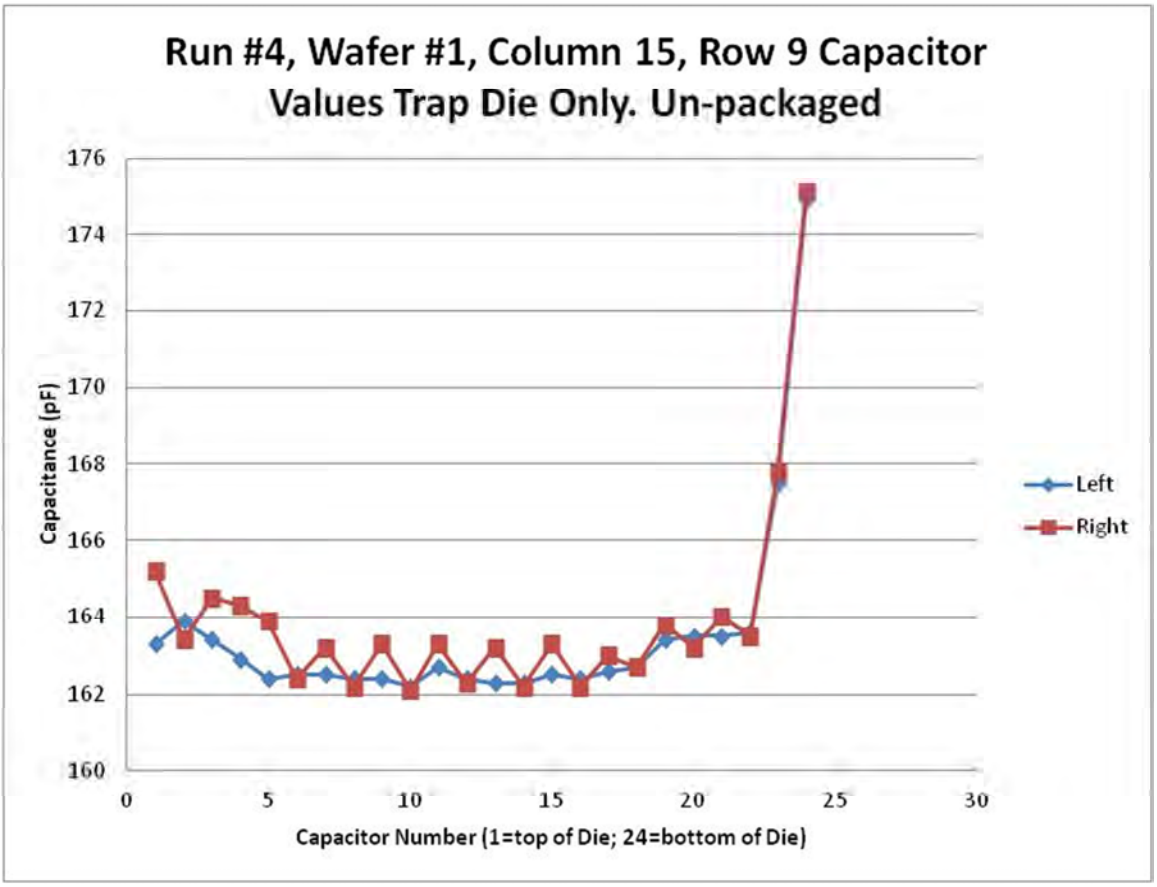


Figure 43: Measured capacitances of the DC electrodes on Die 15-09. Yield: 48/48 = 100%

As discussed previously, the interposer leads add an additional 5-16 pF, depending on which electrode is being measured. Figure 44 shows the capacitance of the leads from interposer 0-4 (Column 0, Row 4) and the measured capacitance of trap 11-09 (see Figure 40) after it has been assembled with interposer 0-4.

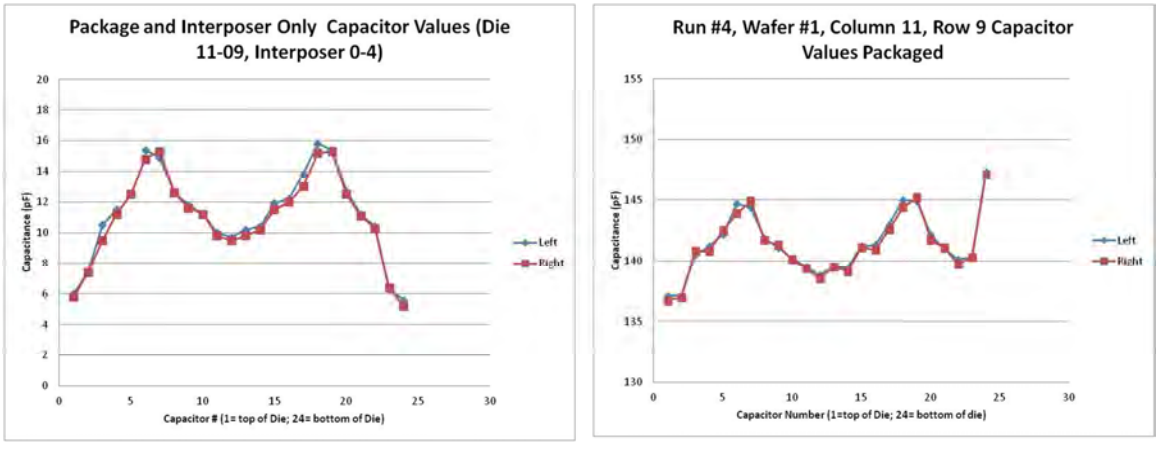


Figure 44: Capacitance of the interposer leads (left) and of a trap after packaging with an interposer (right).

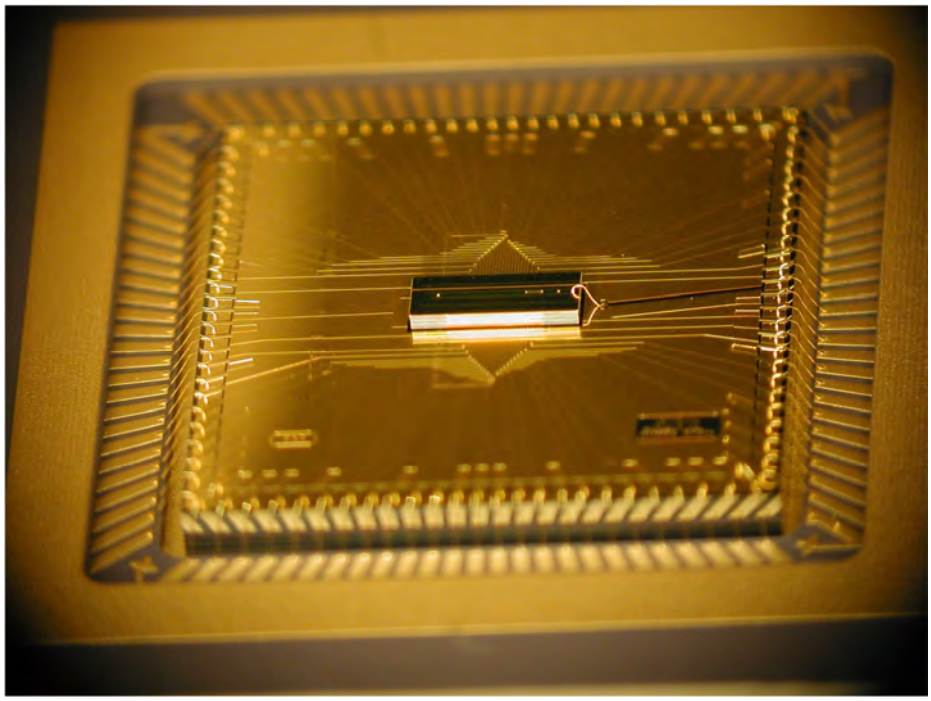


Figure 45: BGA trap. This design used a short bond wire coming up from the interposer to deliver the RF signal.

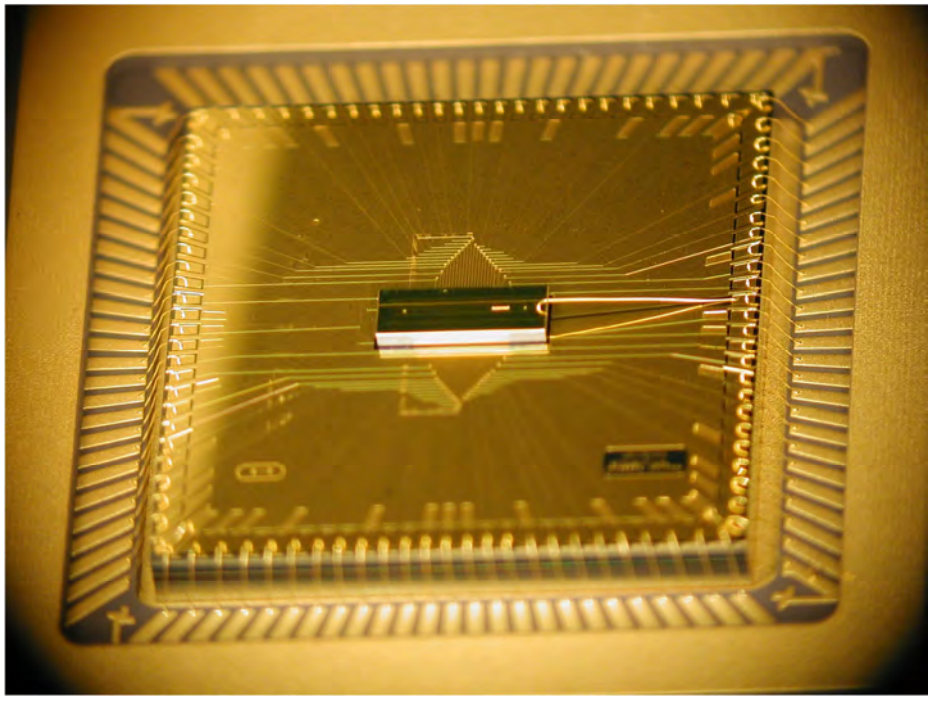


Figure 46: BGA trap. This design used a long bond wire coming directly from the package to deliver the RF signal.

3 Testing

3.1 Overview

A total of 13 trap sets were delivered to GTRI. A set consists of a trap die, an interposer die, and a package, all bonded together. Three of these were considered "perfect" coming out of production, with no known capacitor failures (shorts to ground) or electrode deficiencies. Ten of the traps contained a small but experimentally manageable number of shorts; one such trap was **#04-11**, the primary device characterized in this report.

Trap characterization was performed with BGA trap **#04-11** in the GTRI Ca^+ testing station. This trap contained two electrodes (23R and 17L) that were shorted to ground due to failure of trench capacitors. This trap incorporated a long bond wire for the RF as shown in Figure 46. Key parameters and results from trap testing are summarized below and described in detail in Sections 3.2-3.4. Overall performance judged by these metrics is comparable to or better than previous GTRI surface electrode ion traps.

a. Trap RF: 190 Vpp at 55.14 MHz
b. Axial mode frequency: 1.0 MHz
c. Radial secular modes: 4.2 and 3.7 MHz (Mathieu parameter $q \approx 0.2$)
d. Ion storage lifetime: several hours with Doppler cooling, 400-500 s in the dark (cooling beam off)
e. Stray axial fields: <100 V/m for positions at least one electrode (60 µm) outside the load zone
f. Axial mode heating rate: 0.21(1) quanta/ms, with negligible increase (to 0.22(2) quanta/ms) if the ion is transported at 0.3 m/s during the heating delay time
g. Axial mode frequency stability: <200 Hz (0.02%) over three hours including several ion loss/reload events. Ion reloading causes an additional shift of the axial frequency at the 0.01% level, which persists for 5-10 minutes after loading.
h. Single-qubit rotation rate increased to >250 kHz by focusing of 729 nm gate beam to a waist radius < 10 µm
i. Two ions trapped and reliably co-transported out of the loading zone
j. Two ion storage lifetime of typically 1-2 hours with Doppler cooling, 30-40 seconds in the dark
k. Two ion center-of-mass and stretch axial modes identified and cooled near motional ground state
l. Qubit decoherence time measured at ≈200 µs, limited by magnetic field stability
m. Two-qubit entangling gates demonstrated with fidelity reaching the entanglement threshold (50%), limited by environmental magnetic field noise

Based on encouraging early results from testing of BGA trap **#04-11**, GTRI selected a second BGA trap (**#08-09**, with no known electrical failures) for installation in a Yb trapping station. This station is designated for experiments with two-qubit Raman gates under the IARPA MQCO program. Yb ions have been successfully trapped in the BGA trap, with initial results described in Section 3.5.

3.2 Basic Ion Trap Characterization with Ca^+

We benchmark BGA trap **#04-11** by trapping $^{40}Ca^+$ ions. Trap RF is applied with 95 V peak at 55.14 MHz. Axial trapping potentials are set to give an axial mode frequency of 1.0 MHz. Radial modes are measured at 4.2 and 3.7 MHz. The Mathieu stability parameter is q≈0.2. The experiments below are performed with the ion at z = 488 µm, chosen to be roughly halfway between the edge of the loading slot and the first shorted electrode in trap **#04-11**.

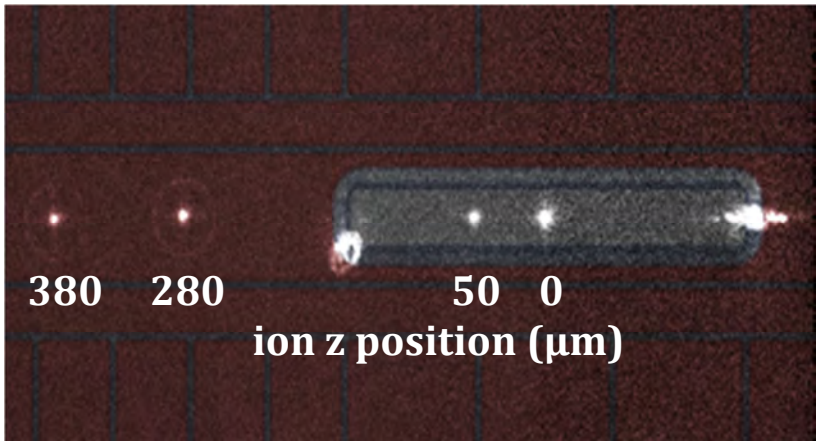


Figure 47: Single Ca+ ion fluorescence images at various locations in the BGA trap. Additional bright features are due to scattering of the trapping lasers off edges of the loading slot and the RF wirebond (far right).

A 397 nm laser is used for Doppler cooling and state detection on the $^2S_{1/2} \rightarrow {}^2P_{1/2}$ transition. Fluorescence at this wavelength is collected onto a CCD camera and a photomultiplier tube; typical camera images of a trapped ion are shown in Figure 47. An 866 nm beam repumps ions that fall out of the cooling cycle into the $^2D_{3/2}$ level. With the Doppler cooling beam on, storage lifetime for the Ca^+ ion is several hours. With the Doppler cooling beam mechanically shuttered, the ion dark lifetime (50% average survival fraction) is ≈ 450 s (Figure 48).

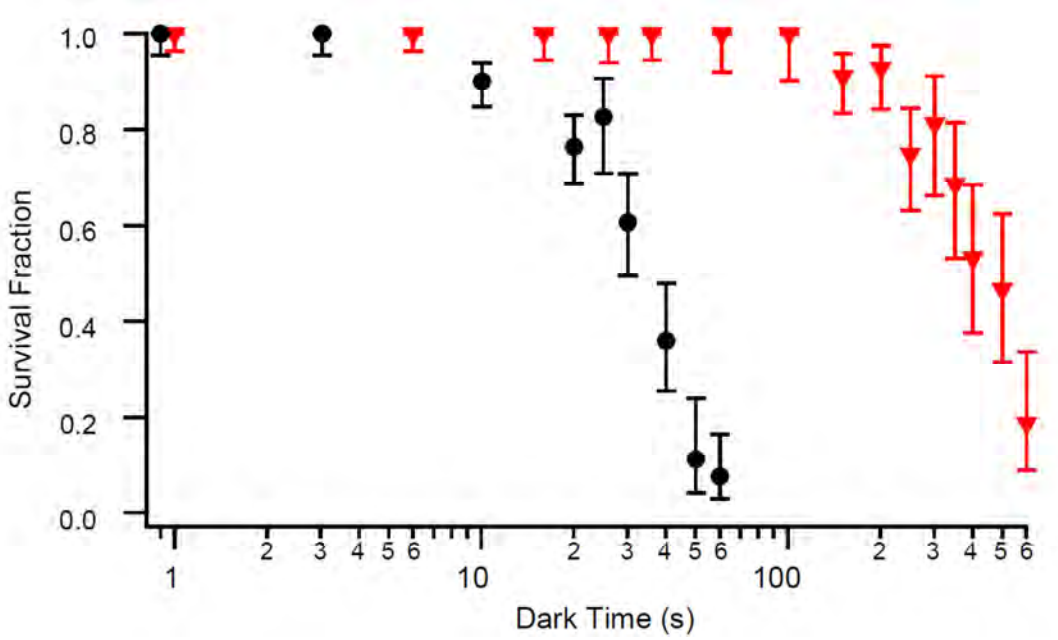


Figure 48: Ion lifetime measurement without Doppler cooling. The dark lifetime (50% survival fraction) is 450 sec for a single ion (red triangles) and 35 sec for two co-trapped ions (black circles).

By measuring shifts in the ion equilibrium position as we scale the harmonic trapping potential, we map out electric field strength E_z over the length of the trap. The resulting map, Figure 49, serves as a measurement of stray electric fields and a test of electrode connectivity. Stray fields near the load zone edge reach several hundred V/m but drop well below 100 V/m after one electrode separation (60 µm) from the load slot. Despite the two shorted electrodes in this trap, we are able to control the ion over the full range z = 0-1200 µm. Stray fields are comparable to those measured in earlier GTRI Gen II and Gen V traps[2,4].

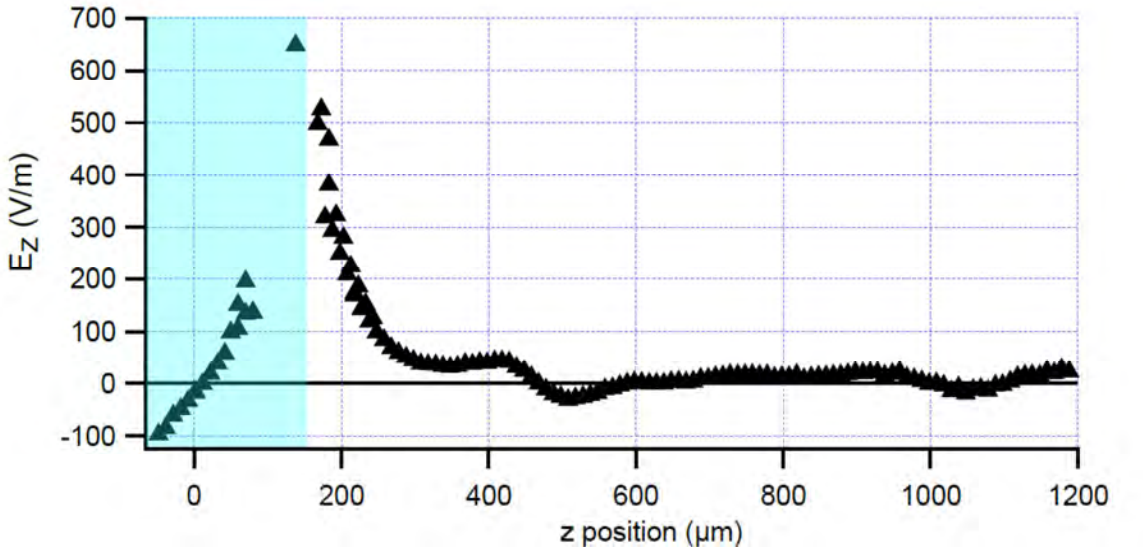


Figure 49: Stray axial field E_z measurements over the BGA trap. Light blue box indicates region of the loading zone.

Relevant to qubit operations for quantum computing, we investigate motional modes of the trapped ion around a motion-independent carrier frequency. The chosen carrier is an electric

quadrupole transition, $^2S_{1/2}$ m_s=-1/2 → $^2D_{5/2}$ m_s=-1/2, with wavelength 729 nm. We apply a weak magnetic field of ≈3 gauss to split the Zeeman sublevels. Figure 50 shows the spectrum around our carrier transition, measured using an electron shelving technique. Axial sidebands of 1st order (f_z=1 MHz) and 2nd order (f=2f_z) are clearly resolved along with sidebands at the radial secular frequencies 4.2 MHz and 3.7 MHz.

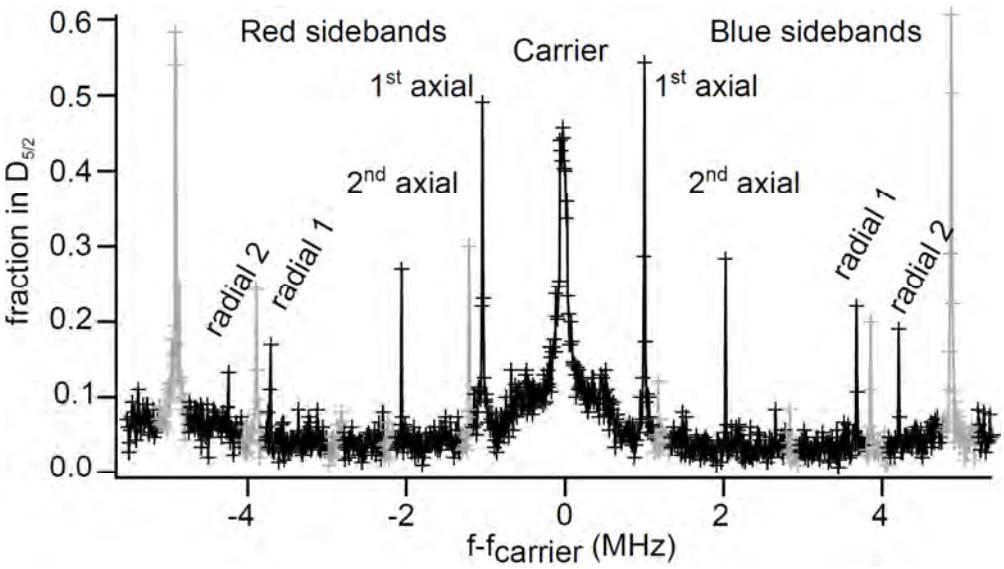


Figure 50: Carrier transition and motional sidebands for a trapped Ca^+ ion as a function of the 729 nm laser frequency. Gray peaks are due to adjacent carrier transitions (between different Zeeman sublevels) and their sidebands.

The carrier transition frequency shifts in direct proportion to applied magnetic field strength. Various technical upgrades to the GTRI testing station were made during this program to improve operations on the 729 nm transition:

1) A clamp assembly, custom machined from aluminum, was added to mechanically secure the trapping chamber to the optical table, reducing relative motion between the ion and the 729 nm laser beam.
2) A feedback circuit was added for optional intensity stabilization of the 729 nm laser. The setup is identical to standard stabilization of our fluorescence detection beams at GTRI: we pick off a small portion of the light for measurement and apply feedback to an AOM in the beam path to maintain constant intensity.
3) To minimize variation in the magnetic field, an active compensation coil was installed. The compensation coil is coaxial with the main B field coil that determines the 729 nm transition frequency, but significantly larger in diameter and farther from the trap. The effective field produced by this coil at the ion location is roughly 0.6 gauss/amp (compared with 1.1 gauss/amp from the main coil). A field probe is placed directly outside the trap chamber to measure stray B field variation near the ion location. Drive current in the compensation coil is then set via feedback to stabilize the probe reading. This system succeeds in nulling out large-scale variations due to 60 Hz line noise. Faster noise components (1 kHz and above) remain uncorrected due to limited frequency response of the field sensor.

We measure stability of the axial mode by repeatedly scanning over the 1st axial red and blue sideband transitions (labeled "1st axial" in Figure 50). The measured axial mode frequency remains within a range of 200 Hz (0.02%) over three hours (Figure 51). We are able to resolve small shifts due to ion reload events, as may result from charging of the trap surface by the load beams. As seen in Figure 51, these reload events typically cause a small (0.01%) increase in axial mode frequency, which then decays over 5-10 minutes.

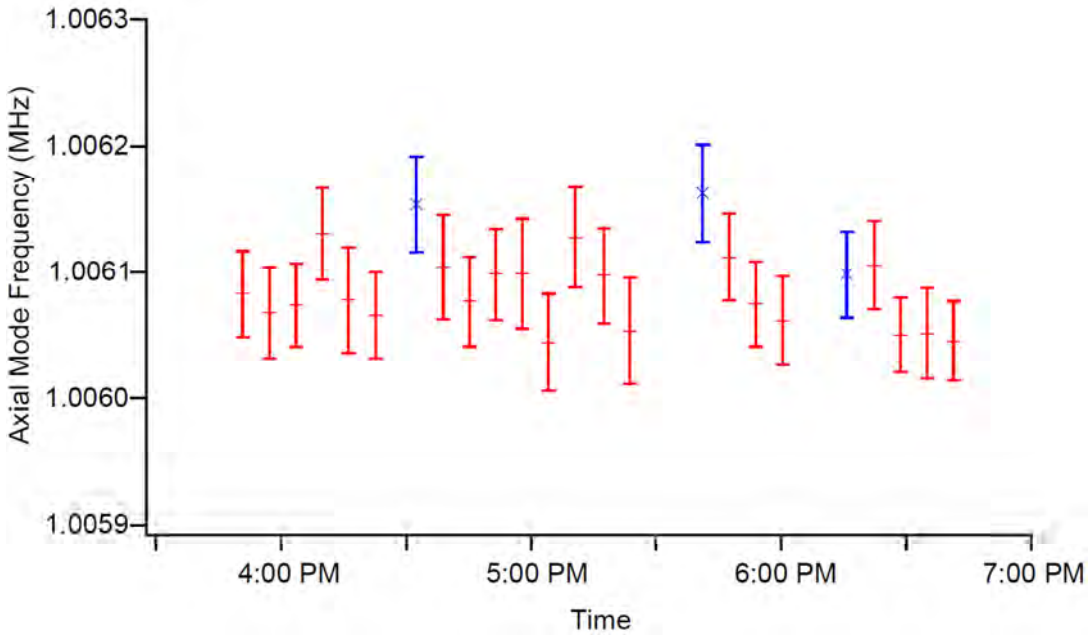


Figure 51: Axial mode frequency stability. Blue points indicate measurements following an ion loss and reload event.

Over a span of two days, axial mode frequency remains consistent at the 0.02% level (Figure 52), though we observe an unusually large settling time after the first ion load of the morning. (During the overnight break, trap voltages are left configured for a trapping well in the load zone, while lasers, magnetic field, and trap RF are turned off.) These results indicate good repeatability of the DC trapping potentials, but the observed charge-up effects suggest allowing a settling time of a minimum of 5-10 minutes before acquiring any critical data after an ion reload.

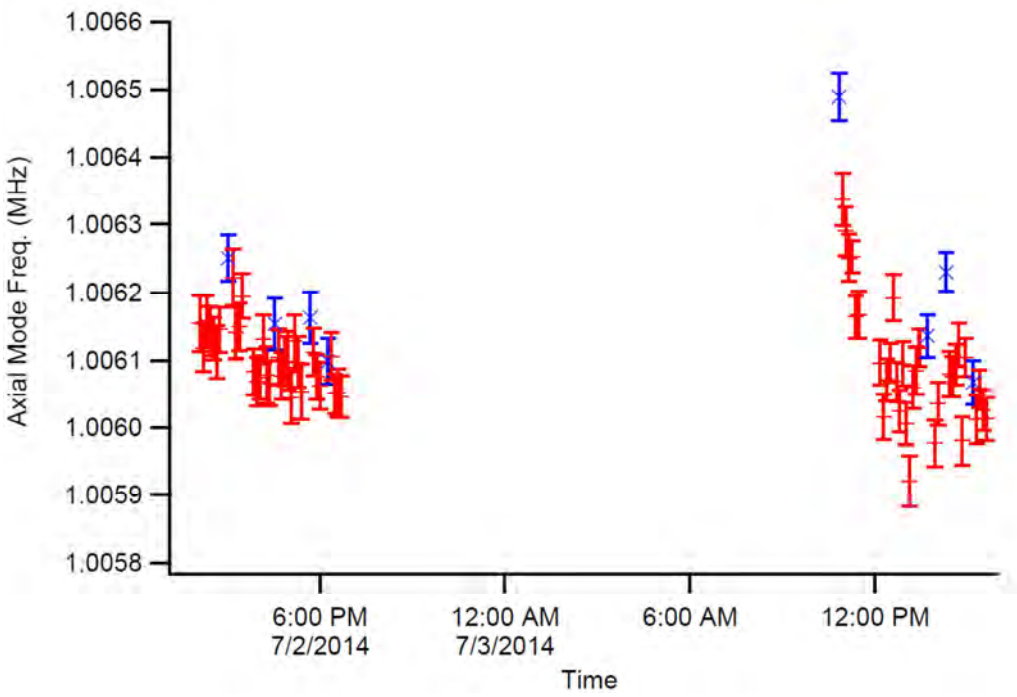


Figure 52: Axial mode frequency stability over two days. Blue points indicate measurements following ion reload.

Ion axial heating is measured following sideband cooling to an average phonon occupation number of $n_{avg} \approx 0.25$ in the axial mode (f_z=1 MHz); n_{avg} is determined by comparing strengths of the 1st axial red and blue sidebands. The ion is allowed to sit without any active cooling for some controlled delay time, then n_{avg} is remeasured to determine the heating rate. Results of this measurement are shown in Figure 53. A weighted linear fit to the data gives a heating rate of 0.21(1) quanta/ms. To check for additional heating due to ion transport, we repeat the experiment with continuous transport of the ion during the delay time. The transport rate is 0.3 m/s over a 300 µm region of the trap (round trips between z=488 µm and z=788 µm). Transport of the ion in this manner does not significantly affect the measured heating rate (blue points and fit in Figure 53).

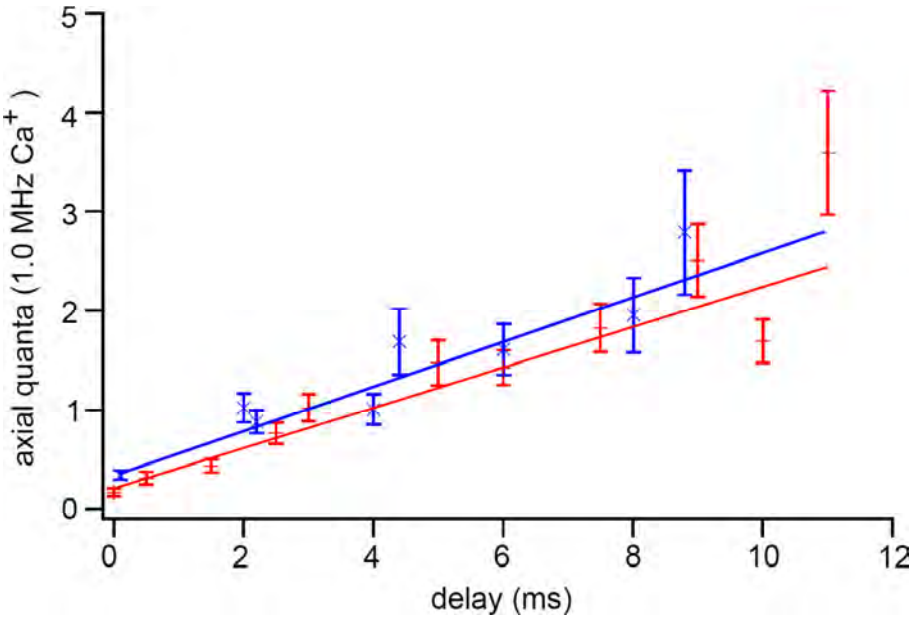


Figure 53: Heating rate of the axial motional mode. Blue points are with transport at 0.3 m/s during the delay time. The resulting heating rate is 0.21(1) quanta/ms without transport and 0.22(2) quanta/ms with transport.

3.3 Gate Beam Focusing for Single Qubit Rotations

A key advantage of the BGA architecture is the possibility to focus laser beams more tightly on the ion. Tighter focus of a gate beam can speed up qubit rotation times by increasing intensity at the ion while also reducing crosstalk to neighboring ions. A focused Gaussian beam will diverge in inverse proportion to ultimate beam waist; that is, a beam tightly focused above the trap surface will exhibit large angular spread as it enters and exits the trapping region. The dimensions of the trap chip and carrier thus present a limit to how tightly we may focus the beam before starting to scatter off some surface at the edges.

We use various lens combinations to focus our 729 nm gate beam onto the trapped ion. The carrier Rabi rate for single qubit rotations is proportional to amplitude of the driving electric field (or square root of laser intensity) at the ion. We measure the laser beam profile by translating the ion while holding the 729 nm laser fixed; beam waist radius is defined as the $1/e^2$ half-width of intensity profile. Results for four different beam waists are shown in Figure 54. The 729 nm beam is incident at 45° to the trap axis, giving rise to a factor of √2 between the physical beam waists and the effective beam waists as measured by this technique. In the following discussion, beam waists refer to the physical values unless otherwise specified.

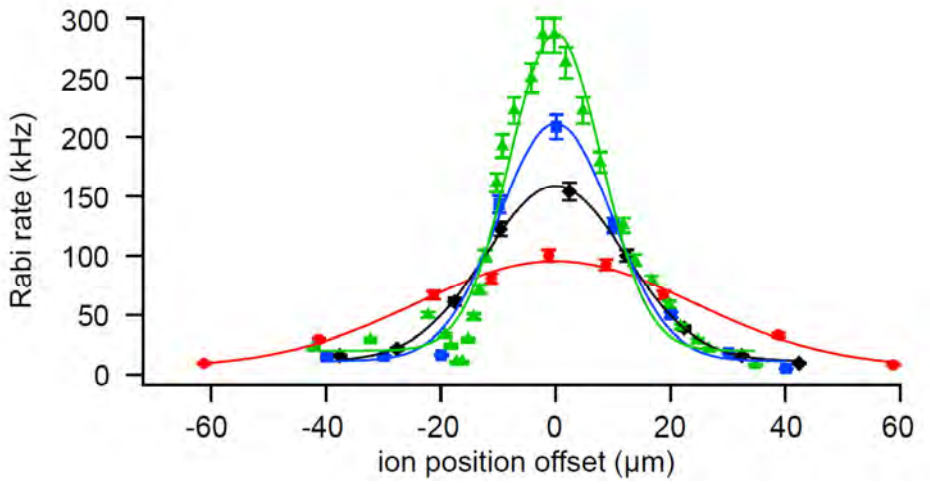


Figure 54: Effect of 729 nm gate beam focus on single qubit transition rate. Correcting for the 45° angle of incidence, the gaussian fits indicate beam waist radii of 24.1 μm (red), 12.2 μm (black) , 9.9 μm (blue), and 8.0 μm

To confirm the beam waist measurements, we use a beam profiler to measure the collimated input beam, then model the layout of focusing optics to calculate effective beam waists at the ion. Results from these calculations are in good agreement with the measured values (Figure 55).

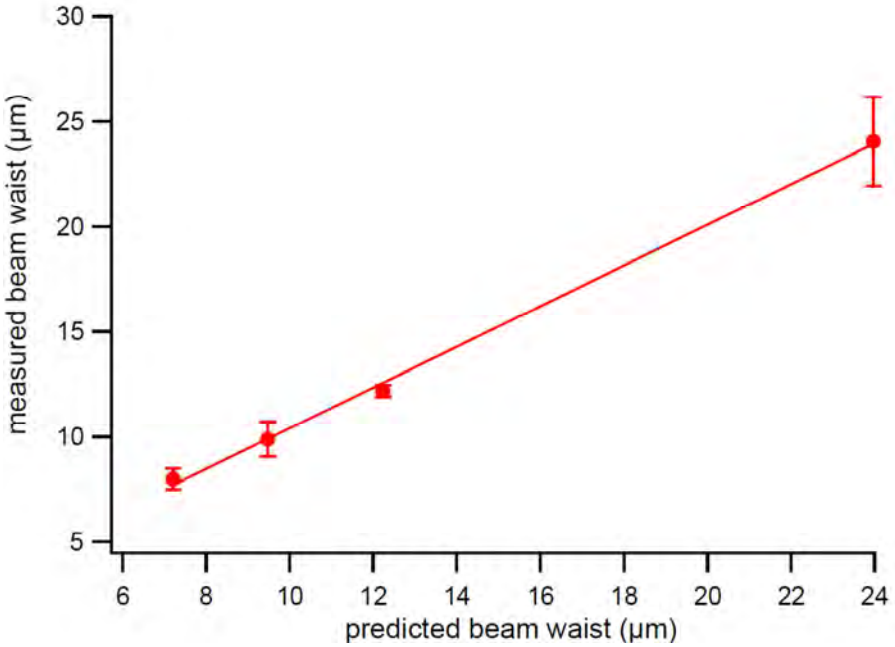


Figure 55: Comparison of 729 beam waists as measured by the trapped ion and predicted by an optical model.

We have assumed constant power in the 729 nm beam and also perfect alignment of its focus on the ion, which is nontrivial as the beam waist decreases. We test these assumptions by checking the scaling of peak Rabi rate with beam waist. Figure 56 shows good agreement between values measured by the ion and predictions derived from our optical model assuming a constant total beam power. We use the peak Rabi rate at weakest beam focus (red in Figure 54), which is the least susceptible to alignment errors, to specify total beam power in the model.

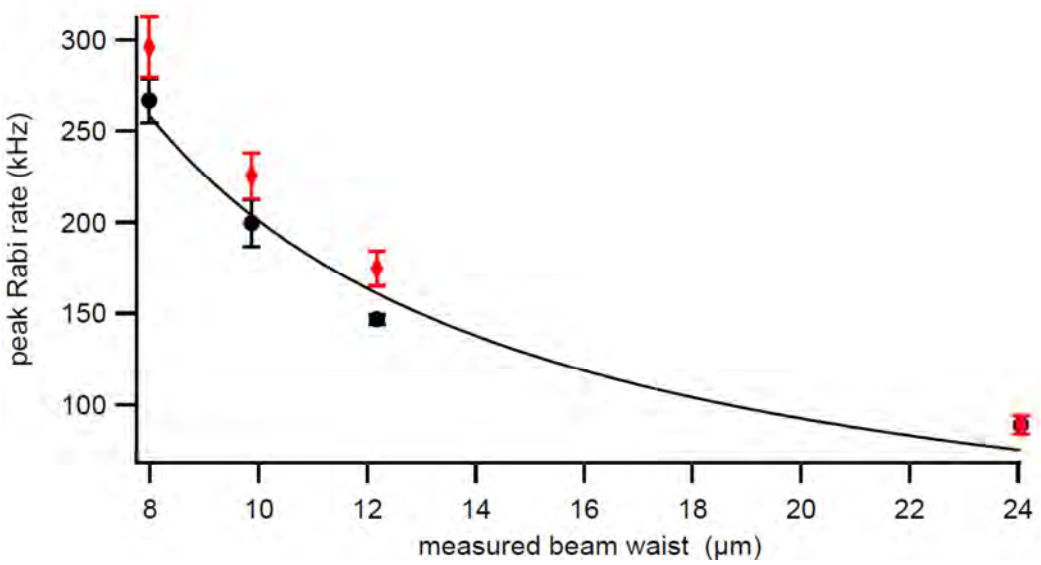


Figure 56: Peak Rabi rate vs beam waist of the 729 nm gate beam: Black points are measured values from Figure 55; red points are predicted values. The black curve represents a constrained power-law fit to the measured data, consistent with expected scaling Rabi_Rate ~ 1 / Beam_Waist.

The tightest waist achieved here represents the approximate limit of beam focusing over the BGA trap; at 8 μm beam waist we are beginning to clip off the CPGA carrier edge, resulting in a loss of a few percent of the beam power. Deviations from the gaussian fit are evident in the wings of the 8 μm beam (green in Figure 54), indicating beam distortion. Beam waists of 10 μm or larger, meanwhile, experience less than 1% power loss due to scattering. As shown in Table 1, such tight beam focusing far exceeds what would be achieved with the same optics in a previous surface trap design (GTRI Gen V trap[4]).

729 nm gate beam waist (μm)	Power loss due to scattering in BGA trap	Power loss due to scattering in GTRI Gen V trap
24.1	$< 10^{-8}$ %	4 %
12.2	0.05 %	17.3 %
9.3	0.6 %	23.6 %
7.4	3.1 %	29.6 %

Table 1: Calculated power losses due to scattering of a Gaussian beam off the BGA trap as characterized here (column 2) and off an older GTRI trap if placed at equivalent position in the vacuum chamber (column 3).

3.4 Studies with Two Qubits

Using the same trap parameters as for a single ion, we load chains of up to six ions (Figure 57) in a single potential well. After calibrating our transport waveforms to correct for stray electric fields in the **z** direction (Figure 49), we are able to reliably co-transport multiple ions out of the load slot to our experiment zone at z = 488 µm. Transport success rates are essentially 100% for co-transport of two ions at speeds of 0.33 m/s or slower. Co-transport of three ions under identical conditions also succeeds reliably (10 successful transports in 10 attempts).

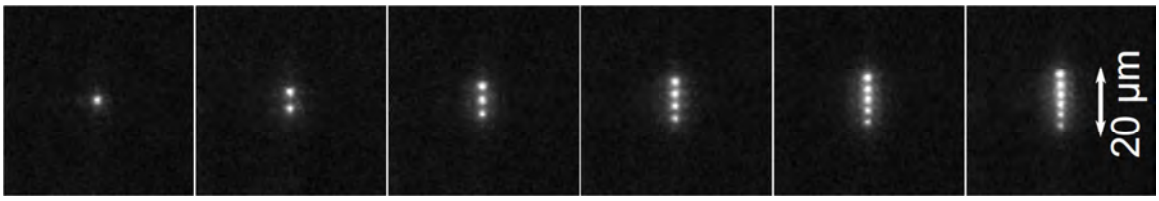


Figure 57: Fluorescence images in the loading zone of one to six trapped ions.

In the experiment zone at z = 488 µm, the two-ion storage lifetime with Doppler cooling is typically 1-2 hours, with a dark lifetime of 35 seconds without cooling (Figure 48). Note that for a two-ion chain we define lifetime by the loss of either ion. The two-ion center-of-mass (f_z=1.0 MHz) and stretch (f=1.73 MHz) axial modes are identified (Figure 58) and cooled via sideband cooling to near the motional ground state, $n_{avg} < 0.25$ quanta in each mode.

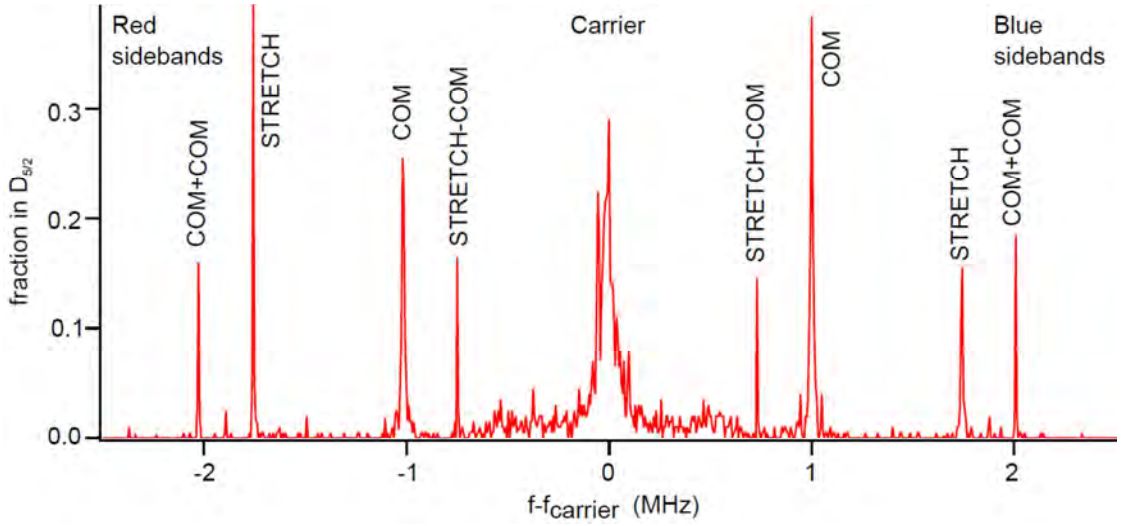


Figure 58: Carrier transition and motional sidebands for two co-trapped Ca+ ions as a function of the 729 nm laser frequency.

To test two-qubit entanglement in the BGA trap, we explore a Mølmer-Sørensen gate operation. The Mølmer-Sørensen gate[5] involves illuminating two co-trapped ions with bichromatic laser light; in our case this driving field has components near the red and blue stretch axial sideband frequencies (see Figure 58). An ideal Mølmer-Sørensen gate (Figure 59a) will take an initial two-qubit state |00> to a final entangled state $(1/\sqrt{2}) \times (|11\rangle - i|00\rangle)$. The interaction time for optimal entanglement is determined by the Rabi frequency and the detuning of the bichromatic driving fields from the stretch mode sidebands.

Figure 59 compares a Mølmer-Sørensen gate operation in the BGA trap with an ideal mathematical model. The gate evolution plots (Fig. 59a-b) indicate total average populations of ions bright (in state |0>) and dark (state |1>); these populations are denoted P_0 for both ions dark, P_1 for one ion bright, and P_2 for both ions bright. The 729 nm gate beam detuning and intensity are adjusted experimentally to produce the gate demonstration shown in Fig. 59b. To generate the corresponding mathematical model (Fig. 59a), we set detuning parameter equal to the known experimental value, then fine-tune the Rabi frequency parameter within experimental uncertainty to optimize $P_2 + P_0$ overlap at 200 μs.

To test for entanglement, we execute the gate operation for 200 μs, then analyze the resulting state by applying a π/2 pulse to the two ions before measuring state populations. Scanning the phase of the analyzing pulse, the measured parity (P_0+P_2-P_1) is observed to oscillate with a period of π radians. The fidelity of the Mølmer-Sørensen gate operation is then calculated[6] as

$$F = \frac{1}{2}(P_0 + P_2 + A) \ ,$$

where P_0 and P_2 are the measured populations at the gate time of 200 μs (from Figure 59b) and A is the amplitude of the measured parity oscillation (from Figure 59c). For the gate operation shown here, we obtain

$$F = \frac{1}{2}(P_0 + P_2 + A) \ = \ \frac{1}{2}(0.822 + 0.202) \ = \ 51.2\% \ .$$

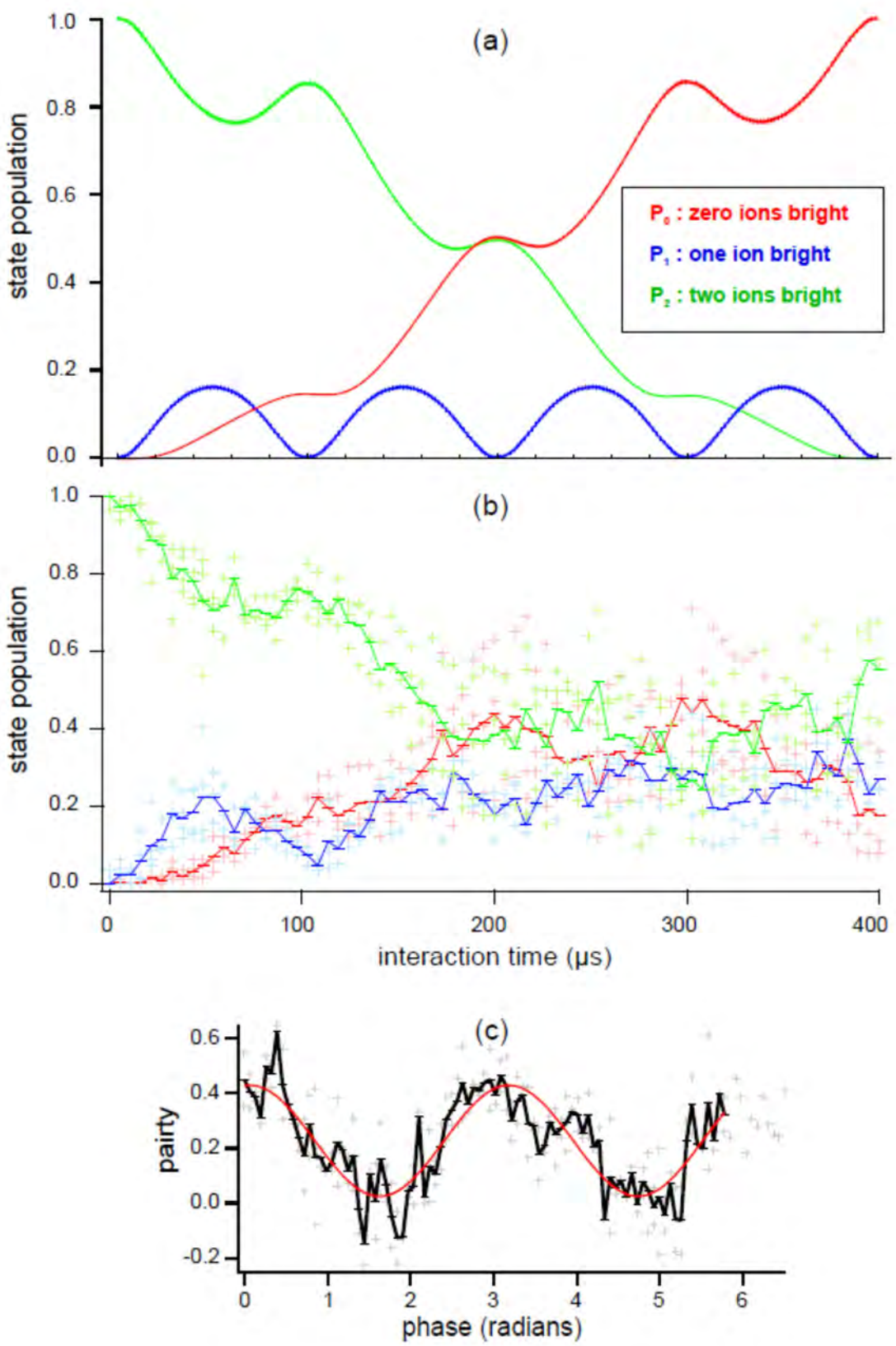


Figure 59: (a) Ideal Mølmer-Sørensen two-qubit gate operation for 10 kHz detuning. (b) Observed gate operation in BGA trap. Deviation from the model at long interaction times is attributed to decoherence caused by magnetic field fluctuations. (c) Parity measurement at 200 μs interaction time.

Experimental uncertainties prevent us from making an unambiguous claim of two-qubit entanglement, which requires fidelity greater than 50%. In particular the measured ion state populations exhibit considerable drift between experimental runs; the lighter points in Figure 59b-c indicate individual data traces that were averaged together to form the solid line plots. The observed gate operation (Figure 59b) also deviates increasingly from the model (Figure 59a) as the interaction time grows longer. These effects are consistent with the qubit decoherence time scale of 200 μs that we measure using a Ramsey technique. We attribute this decoherence primarily to magnetic field fluctuations. The 729 nm qubit transition is field sensitive; the trap testing station has no magnetic shielding and active field stabilization only at low frequency (< 1kHz). However, the results obtained here bode well for future two-qubit operations with Ca^+ ions. A likely candidate for one of the remaining BGA traps is GTRI's Physics station, a magnetically shielded station intended for precise gate operations. Coherence times exceeding 1 ms were recently measured for the 729 nm transition in the Physics station.

3.5 Yb^+ Trapping in MUSIQC Station

BGA trap **#08-09** was installed in GTRI's MUSIQC trapping station in July 2014. The MUSIQC station is designated for multiple-ion operations under the IARPA MQCO program with $^{171}Yb^+$ ions. Gates on the $^{171}Yb^+$ hyperfine qubit use a pulsed 3x YAG laser with ≥ 100 mW per beam at 355 nm. The high powers in these beams represent a different operating regime for this trap compared to the $^{40}Ca^+$ testing. Additionally, the $^{171}Yb^+$ hyperfine qubit is first order magnetic field insensitive, removing the magnetic field noise that limits the $^{40}Ca^+$ gates (see Section 3.4).

During initial characterization of the BGA trap in the MUSIQC station, we found that the RF rail was only capacitively coupled to the RF source. Without DC connectivity, electron field emission from the RF rail caused the rail to charge to a few volts bias that depended on the RF amplitude. Once charged, the rail would take tens of minutes to discharge. This bias caused instability in the radial mode frequencies.

Further investigation showed that the interposer used for the RF bond wire configuration in Figure 45 had a missing oxide etch that left the RF wirebond pad on the interposer disconnected from the RF trace. The trap was repaired with a single wirebond from the pad to the edge of the interposer to complete the connection.

With the repair in place, we quickly characterized the radial modes for single ions and chains of two to four ions and demonstrated a ~90 % Mølmer-Sørensen gate on two ions (Figure 60). The fast gate operation is aided by the tight gate beam focusing afforded by the BGA.

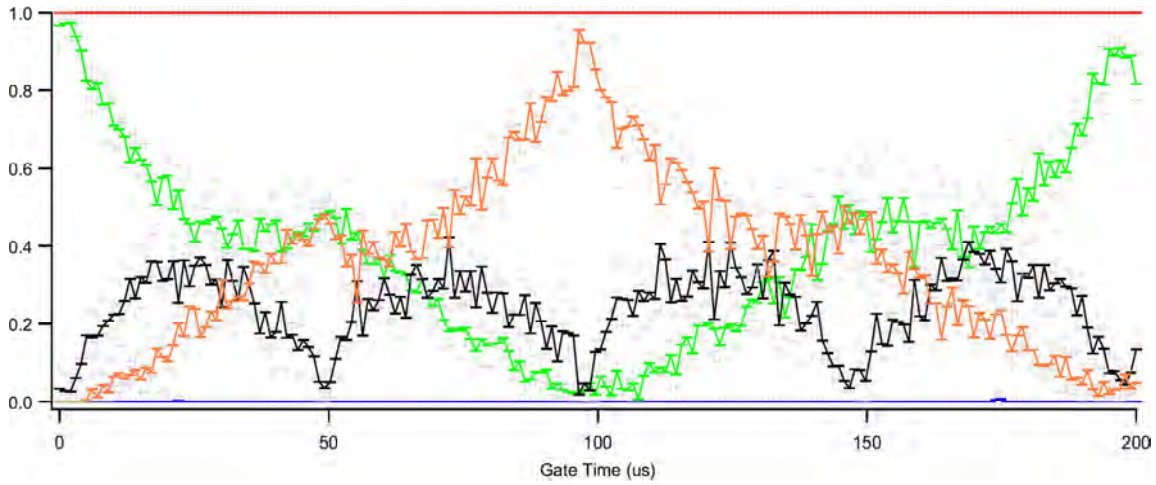


Figure 60: Mølmer-Sørensen gate on two $^{171}Yb^{+}$ ions. Plot shows the fraction of measurements with zero (green), one (black), and two (orange) ions bright. The gate completes at 50 µs with a 90 % state fidelity. By the full 200 µs of the scan, the ion pair has undergone four Mølmer-Sørensen gates.

4 Optics Integration Study

4.1 Introduction

Prior Optical Integration Efforts

State of the art experiments in ion trap quantum computing involve the delivery of free-space laser beams through optical windows to address the ion in the trap. Alignment of optics inside vacuum chambers is typically expensive and cumbersome. Large dielectric surfaces can become charged by trapping fields and laser light, so they are rarely incorporated inside the vacuum chamber. Since integrated optics are not necessary to perform most fundamental physics experiments, there has been only limited experimental development of concepts to date. Here we summarize some of those concepts.

A concept for integrated laser delivery investigated at Sandia National Laboratory uses single-mode fibers mounted in ceramic ferrules. These ferrules are tipped with diffractive lenses and epoxied onto the backside of the ion trap. Light can then either irradiate an ion directly through a slot in the trapping zone (Fig. 61) or indirectly by a beam parallel to the surface created by reflection off an angled mirror. This integration was attempted, but there have been no successful demonstrations to date.

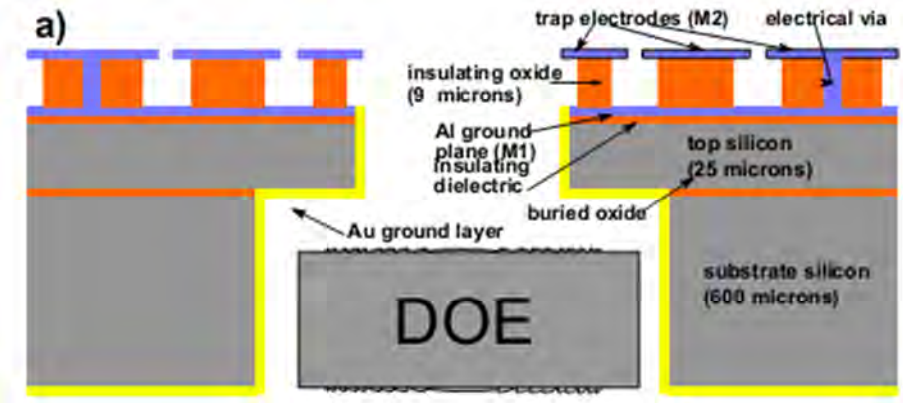


Figure 61: Representation of direct illumination of an ion by an integrated DOE/Fiber (fiber not shown). Reference: arXiV 1305.4706v1

Another concept uses off-axis diffractive mirrors imprinted into the trap surface [DTIC ADA606612]. Beams normal to the surface are reflected at an oblique angle towards a nearby ion. Very tight beams (< 1 µm waist) should be realizable with this approach. However, a lot of light will be absorbed or scattered by the diffractive mirror. These optics have been manufactured, but have not yet been tested.

Optical Cavities

A second potentially interesting design is the integration of moderate to high cooperativity optical cavities. The cavity enhances the collection of scattered light from the ion, which enables faster readout and remote entanglement via entangled photons. The requirement of small

mode volume for these cavities means that they must be located inside the vacuum system very close (~100's of microns) to the ion. The alignment of the cavity mode to the ion must typically be done to much better than 1 μm. A number of academic teams have shown results with cavities and ions. Typically, these involve large 3D traps with large, independently mounted mirrors. A few efforts exist to integrate the cavity with the trap itself.

Concepts explored to date include:

- Fabricating the trap directly on the tip of a fiber with a high-reflectivity coating (MIT, Duke). The second mirror is suspended above the trap and is not necessarily integrated with the trap. This does not represent a scalable system. Fabrication techniques have been explored for making the trap on the fiber tip, but we are not aware of a complete system under test.
- Fabricating the cavity mirrors directly on the tip of a single mode fiber, which is then positioned in a slot in a microfabricated ion trap (Schmidt-Kaler). There is no evidence that any real efforts have been made beyond conceptualization. The length and position of the cavity mode are not adjustable, so this concept is of limited use.
- Attaching mirrors above and below the trap. This approach has been funded at Sandia National Laboratory under the MQCO program. Progress has been made to register the optics to the trap and incorporate piezos for adjustment of cavity length and alignment. Investigations of the stability of the cavity mirror coatings are encouraging. There are no successful demonstrations of this project.

4.2 BGA Program Optical Integration Studies

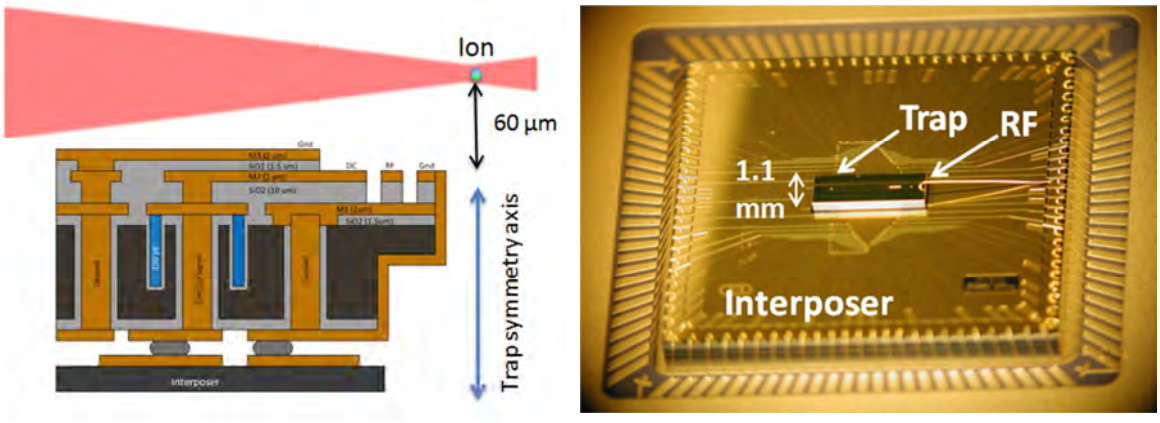
Motivated by the evident need for advanced concepts for scalable optics integration with ion traps, the SMIT BGA program performers researched concepts for optical integration with the BGA ion trap. This report focuses on the concept of mounting micromirrors on the interposer surface to allow for improved ion addressing and distinct Doppler laser cooling and qubit operation zones. Having micromirrors so close to the ion position will allow for tighter beam focusing and individual ion addressing. Other possibilities could include multiple ion traps positioned on a single interposer die or more intricate trap designs. This discussion covers the necessary architecture and hardware to build a unit cell that would take advantage of the micromirrors on the chip surface. Currently it only takes into account Doppler cooling and qubit operations for Yb^+ ions, though it would be possible to switch atomic species.

Ball Grid Array Architecture

Ion traps use a combination of electrical fields to capture an ion in a potential well. Current state of the art ion traps are space limited due to on-chip filter capacitors and optically limited due to wire bonds in the beam path. As described in the previous sections, GTRI and Honeywell International collaborated to develop a novel ion trap fabricated using Ball Grid Arrays (BGAs).

Moving to the BGA architecture (Fig. 62) results in two major improvements in terms of optics integration. The first benefit of this structure is for full optical access to the trap. Mounting the trap die on the interposer removes the wirebonds from the edges of the trap die and moves

them to the outer edge of the interposer. Full 2π optical access around the perimeter of the trap is now possible because the trap die is raised above the level of the wirebonds. The second benefit of this design is that integrating the filter capacitors onto the trap die with on-chip trench capacitors allowed a reduction in die size by a factor of 30. An immense amount of space is available on the interposer die.



(a) (b)

Figure 62: Pictures of SMIT BGA trap – (a) cross-section schematic showing unobstructed beam path to ion, and (b) picture of actual BGA trap.

BGA Optics Integration

This study focused on two goals – developing a concept to individually address a large number of ions while minimizing the number of lasers and utilizing extra space on the BGA's trap die. The former goal addresses the need for scalability, where the move from single to multiple traps, as in Figure 63, follows a non-linear increase in the number of lasers. Ideally, a single set of lasers could feed many traps (or trapping zones/qubit regions), thereby reducing the supplementary hardware and lab space required. The latter goal aims to place mirrors onto the die surface, an additional design variable that should assist in scalability realization.

To meet both goals, we have outlined the design of Scalable Multiplexors for single-Ion Addressing (SMIA), a system that establishes a non-linear relationship between required lasers and number of traps while utilizing flat mirrors on the die to direct the light. SMIA is split into three separate cells – the first prepares and shutters the laser, the second aligns the laser to the trap, and the third detects the fluoresced light from the ion. The three-part design enables single-ion addressing, for both Doppler cooling (DC) and qubit operations (QO), and single ion detection across multiple traps with a minimized number of lasers. Note that QO includes Raman cooling, state preparation, qubit transitions, and gating.

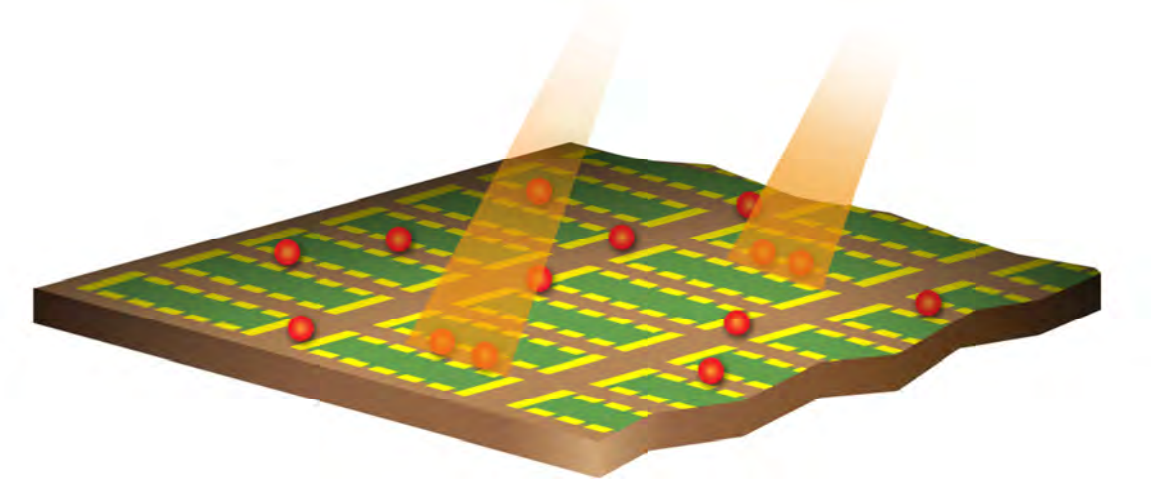


Figure 63: A concept picture showing many BGA traps with multiple ions (red spheres). This type of structure requires optical scalability.

Section 4.3 describes the layout of the SMIA system complete with figures and rough layouts of the three cells. Section 4.4 displays optical modeling results that demonstrate SMIA's basic functionality of coupling light from fibers to the die mirrors and to an ion itself. Finally, SMIA's design assumes the following:

- Ytterbium ions are trapped, meaning that a 369 nm laser with appropriate sidebands[7] may be used for both the DC and QO. The necessary repump lasers are sent axially along the trap from another location and are not considered part of this assembly. Ionization of ytterbium atoms is also performed at a separate location.
- The trap includes integrated micromirrors for increased fluorescence collection, as detailed in *New J. of Phys.* **13** (2011), 103005. Diffractive optics could also be used (See IDM final report, *www.dtic.mil/cgi-bin/GetTRDoc?AD=ADA606612*).

4.3 Scalable Multiplexors for single-Ion Addressing (SMIA)

Scalable Multiplexors for single-Ion Addressing (SMIA) is schematically pictured in Figure 64. Incident laser light is initially split into many components using a fiber bundle. The fibers split and enter the preparation cell, the first of three cells in SMIA's light path, which prepares the light state and shutters the individual beams. Two preparation cells are required, one each for the Doppler cooling (DC) and qubit operations (QO) lasers, since these beams have different preparation procedures. The fibers re-bundle and move into the vacuum chamber. Then, fibers re-split and enter the second cell, the alignment cell, which aligns the individual fibers to the die mirrors and the trap micromirrors. Next, the fibers containing the fluoresced light re-bundle and exit the vacuum chamber. Finally, they re-split before entering the detection cell, the third and final cell in SMIA, which measures the light using an array of photomultiplier tubes.

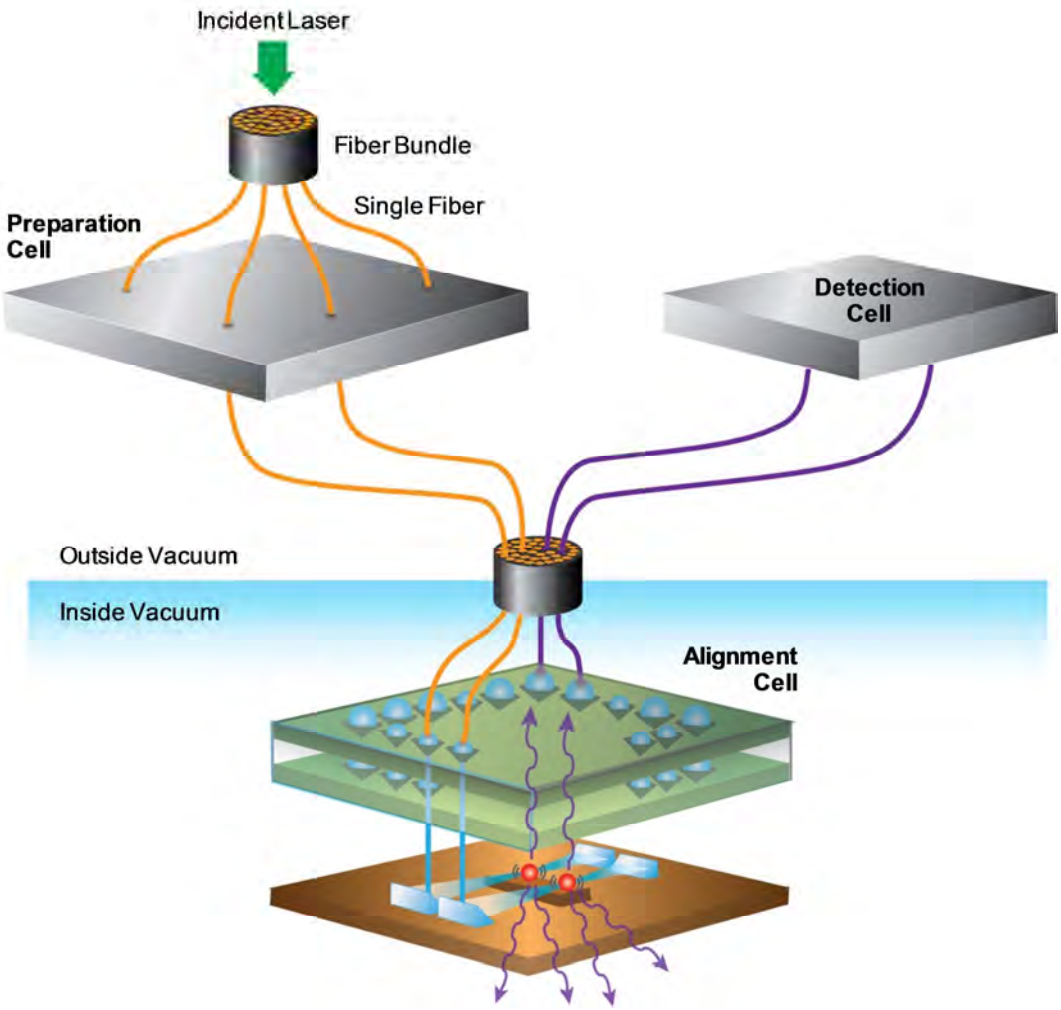


Figure 64: Cartoon of SMIA displaying all three cells and rough light paths. The various cells are described further in the text. The preparation cell corrects for frequency, power, and polarization before the lasers are sent to the alignment cell which focuses the laser light onto the mirrors placed on the chip surface. The mirrors allow for ion addressing and tighter focus than typically seen with standard systems. Emitted photons are collected into fibers again using ball lenses and then sent to individual PMTs. Notes on color: blue is free-space laser light (369 nm for Yb^+), red spheres are ions, and purple arrows are emitted photons. The white shapes on the die surface are flat mirrors.

Scalability of Lasers

The number of ions a single laser can address in SMIA is set by three factors - the power of the illuminating laser, the power required at the ion, and the loss due to the components within the three cells. The main loss stems from the preparation cell and is due to the electro-optical modulator (EOM), acousto-optical modulator (AOM), and Pockels cell path that each beam follows (described further in the preparation cell section). Secondary losses in the other two cells are mainly Fresnel, which are ignored here because we assume that all parts are anti-reflection coated. Then, the total transmission in the preparation cell is

$$\tau_{tot} = \tau_{EOM}\tau_{AOM}\tau_{Pockels} = 0.3 * 0.7 * 0.99 = 0.2,$$

where the numbers are estimated using datasheets from component suppliers. Then, the power at the ion is given by

$$\Phi_{ion} = \tau_{tot}\Phi_{laser}.$$

Finally, the number of ions *N* that a laser can address is

$$N = \frac{\Phi_{ion}}{\Phi_{required}} = \frac{0.2*\Phi_{laser}}{\Phi_{required}},$$

where $\Phi_{required}$ is the laser power required for a given ion operation. Now we can calculate the scalability of the DC and QO lasers. The required power for DC and QO is 1 µW and 10 mW, respectively. Assuming a 1 W 369 nm laser, a DC and QO laser can address $2x10^5$ and 20 ions, respectively. Thus, SMIA features a non-linear relationship for both ion operations, with the DC laser having an extremely large ratio.

Preparation Cell

The preparation cell's function is to generate large spacing sidebands for state preparation and addressing hyperfine transitions using an EOM, to control the laser frequency and shutter the beam using an AOM, and to set the polarization state with a Pockels cell. This arrangement allows not only immense control over every individual beam, but also remote, computational control to remove human-caused errors. Note that all equipment that comprises the preparation cell is currently commercially available.

The preparation cell comes in two varieties for the DC and QO lasers, as detailed in Figure 65, with the main difference being the EOM location. For the DC laser, a 7.37 GHz EOM is needed to avoid dark population trapping. This EOM may be placed before the cell and fiber bundle separation since all DC beams require the same frequency. This is a large reduction in complexity as there is only one EOM instead of N_{DC}. Then, the fiber bundle separates with each fiber passing through its own 200 MHz AOM and Pockels cell, allowing each beam to be individually shuttered and prepared. Light leakage from the AOM shutter, if larger than acceptable, can be further controlled with the addition of an RF switch. The Pockels cell is the final element to avoid the EOM and AOM from disturbing the polarization state.

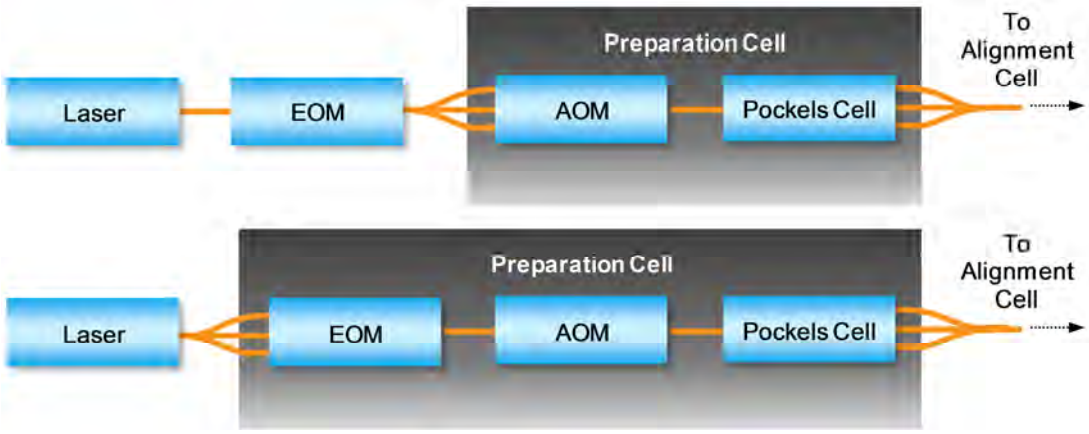


Figure 65: Beam path in preparation cell for (top) DC and (bottom) QO beams. The split arrows indicate a fiber bundle separating. Other labels: EOM = electro-optical modulator, AOM = acousto-optical modulator.

For the QO laser, the EOM moves into the preparation cell and changes to 2.1 GHz as needed for state initialization (the AOM remains 200 MHz). Now, each of the N_{QO} beams has individual control of frequency, as well as shuttering and polarization, allowing for state preparation of individual qubits. This additional step enables each QO beam the ability to set and interrogate ytterbium's hyperfine qubit states.

Alignment Cell

The alignment cell is used to hold and align the individual fibers and their focusing lenses. The alignment cell focuses the input beams on the ion in the trap and collects the ion output fluorescence, focusing it into the output fiber. The alignment cell is designed as a unit cell that can be repeated across a 2D array of traps. As shown in Figure 66, the unit cell is three beams – one each of DC, QO, and Fluorescence Collection (FC). The DC and QO beams are focused at the ion location, and then terminate at a beam dump to mitigate stray light and heating in the system.

Both delivery and collection fibers have a ball lens between the fiber end and the die. For delivery fibers, the lens focuses the beam and directs it towards a mirror on the die surface that directs it at the ion. The lens' focal length is set to garner the correct beam waist and location for the given ion operation. For collection fibers, the ball lens focal length is set to couple the reflected light from the micromirror into the fiber. Furthermore, fluorescence crosstalk can be greatly mitigated by matching the numerical apertures between the micromirror and ball lens.

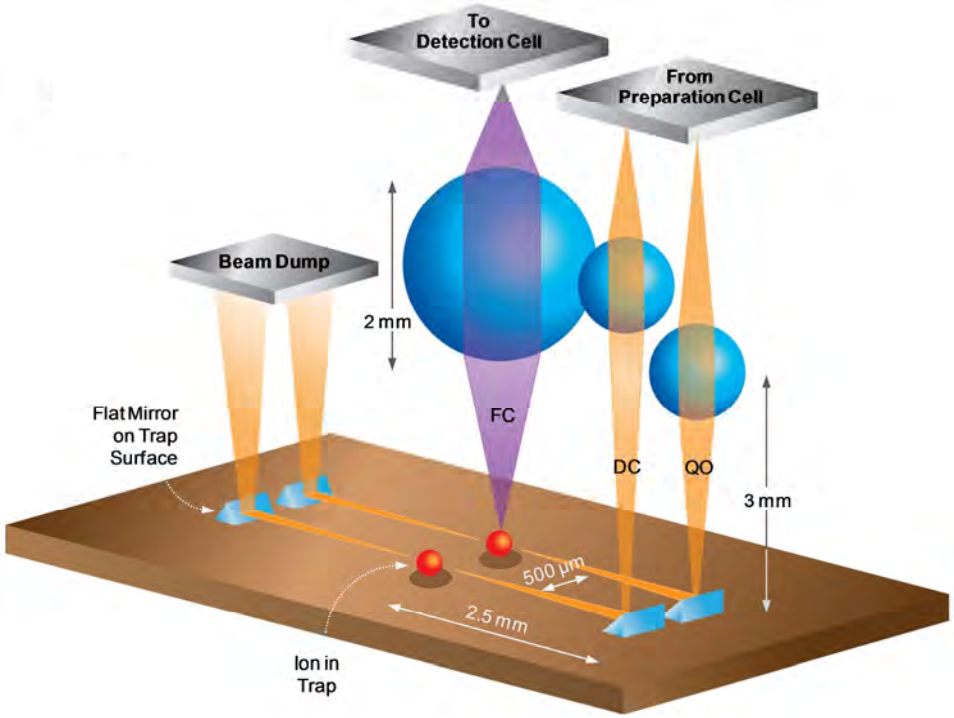


Figure 66: Model of unit cell within the alignment cell. This arrangement can be repeated for an array of traps. Note that the unit cell is inside the vacuum chamber. Labels: FC = fluorescence collection, DC = Doppler cooling, QO = quantum operations, and red spheres = ions.

Alignment Cell Structure and Fabrication

The alignment cell can be fabricated using silicon optical bench (SiOB) techniques developed at Honeywell. SiOB technology employs anisotropic and deep reactive ion (DRIE) etching techniques in silicon. Anisotropic etching is used to create V-grooves for fibers and pyramidal pits for ball lenses to reside, a method that enables precision passive alignment and tolerances between the fibers and ball lenses. DRIE is used to create straight-walled etched structures in

silicon to hold additional optical components such as beam splitters and polarizers to build up increasingly complicated miniaturized optical systems.

Examples of SiOB structures designed and fabricated at Honeywell are found in Figure 67. Figure 67(a) and (b) show a pyramidal pit etched in silicon that holds and self-centers a ball lens, while (c) displays a SEM close-up of a fiber coupled to a ball lens. Figure 67(d) combines the ball lens, fibers, and associated grooves to form a fiber-to-fiber coupler, a self-aligning system that leads to a high coupling efficiency.

As with the preparation cell, all components of the alignment cell (such as the fibers and lenses) are commercially available, and the SiOB technology uses established MEMS fabrication techniques. That being said, a sizable development effort would be required to fabricate the alignment cell on a large scale. The technology, while understood, is being applied to a very different geometry. Figure 67 shows SiOB structures all fabricated in a single plane, whereas the layout of the unit cell of the alignment cell is in three dimensions. The three dimensional structure along with the linking of many unit cells would thus require the development of novel techniques for fabricating and assembling the unit cell.

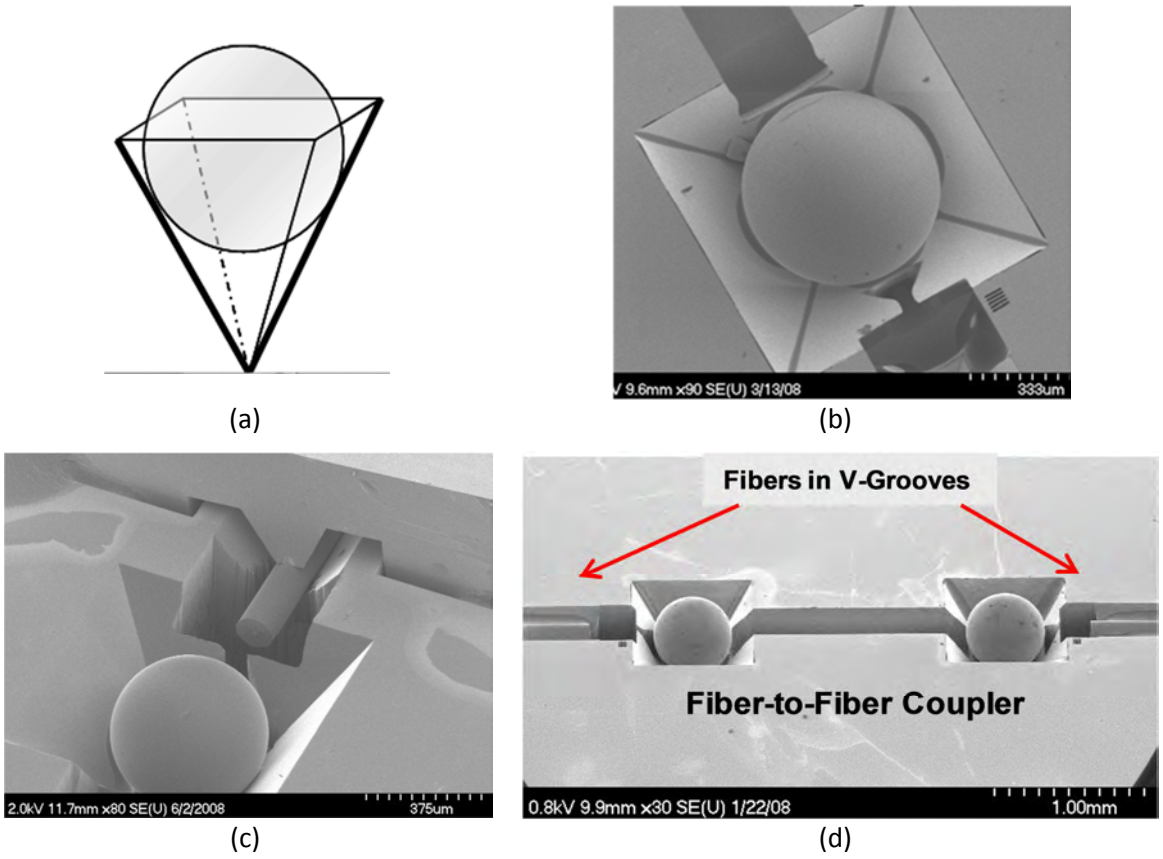


Figure 67: Examples of silicon optical bench structures manufactured by Honeywell. (a) Schematic of a ball lens in a pyramidal pit, (b) SEM picture of a 0.5 mm lens in a pyramidal pit, (c) close-up of a fiber coupled to a ball lens, and (d) a fiber-to-fiber coupler.

An approach for the design architecture and fabrication of the three-dimensional alignment cell is presented in Figure 68. The figure is a cross section along the y-axis of a single trap unit cell

with the trap axis into the page. The figure shows the alignment of the QO fiber and beam to the trap, and also the alignment of the Fluorescence Collection fiber. The DC fiber and lens are out of the page and are not shown in this figure but would be included on the same structure and fabricated in the same sequence.

The alignment cell in Figure 68 is made up of a series of silicon (Si) wafers that are etched, stacked up and bonded together to create structures to hold and align the fibers and ball lenses. There are many variations possible on the fabrication sequence for the alignment cell. The fabrication sequence could proceed as follows:

1. **Si-1 Wafer:** Straight sidewall holes are etched through the first silicon wafer, Si-1, using DRIE. The purpose of Si-1 is to protect the bottom of the ball lenses. A through-hole is also etched for the QO beam to exit to the beam dump. This through-hole is carried through the rest of the wafers. DRIE is used to etch all straight side-walled cuts in the silicon.

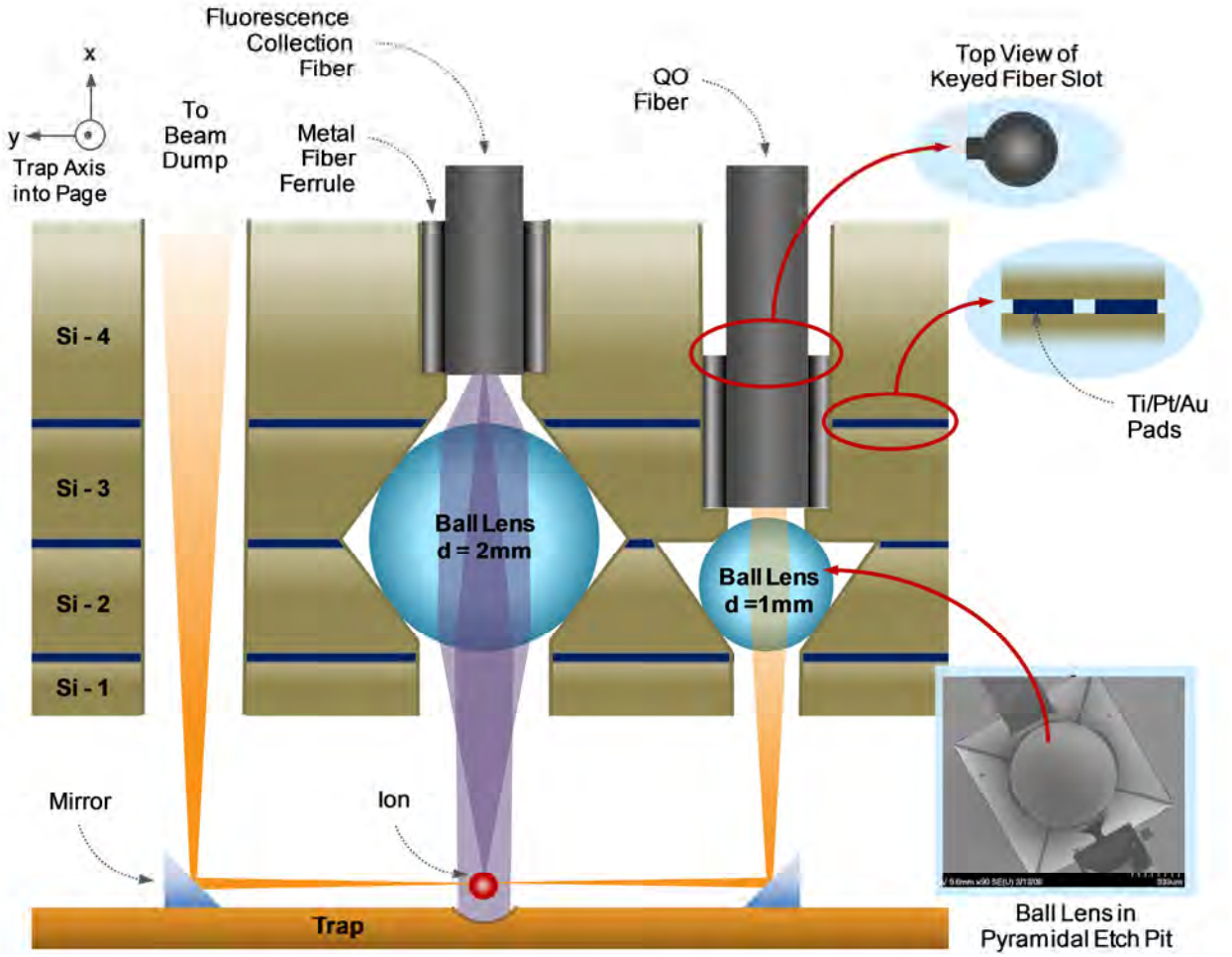


Figure 68: Cross section of a unit cell showing the architecture and alignment of the QO and FC fibers and beams. The figure also shows the beam alignment to an ion trap die. Labels: Si = silicon, QO = quantum operations, and d = diameter.

2. **Si-2 Wafer:** The pyramidal angle-walled structures are etched in Si-2 using anisotropic etching. Anisotropic etching etches along specific crystal planes in silicon to form these angle-walled holes. The main purpose of Si-2 is to create the structures to hold the ball lenses as in Figure 67 and Figure 68. Anisotropic etching is used to create all the angled etched structures in the cell.
3. **Wafer Bonding – Si-2 to Si-1:** The silicon wafers in the stack will be bonded together using an Au-Si eutectic bonding technique. This is done by depositing a metal stack on one of the wafers consisting of TiW/Pt/Au. The metal layer is not continuous and has some channels left in it so that the gaps between wafers will be pumped out in the vacuum system. The second wafer has a bare silicon surface. The wafers are then pressed together in a wafer bonder and heated to a temperature above the eutectic point of Au/Si (370 °C). In order to bond multiple wafers together successively as we will in this stack of silicon wafers (and also attaching the fibers) the first bond must be done at a temperature much above the eutectic point (~450 °C) and then each successive bond done at a lower temperature so that the previous bonds remain intact (e.g., 450 °C, 425 °C, 400 °C, 375 °C).
4. **Si-3Wafer:** The inverted pyramidal structures that will form the covers for the ball lenses are etched in Si-3. DRIE is also used to etch the opening for the QO fiber. The through-hole for the fiber is smaller at the bottom to form a stop for the fiber at a precise distance from the ball lens which will then determine the focal distance from the lens. The shape of the larger opening for the fiber with the metal ferrule will also have a key hole that will match a key on the fiber ferrule. This will align the fiber to maintain the orientation of the beam polarization.
5. **Ball Lens Placement and Wafer Bonding of Si-3 to Si-2:** The ball lenses are placed in their respective lens pit sizes and wafer Si-3 is bonded to Si-2 using the same bonding technique described in Step 3 above. The placement of the ball lenses could be automated using pick-and-place machinery.
6. **Si-4 Wafer Etching and Bonding:** DRIE is used to etch the keyed alignment hole for the FC fiber and the stop for positioning it in its position relative to the collection ball lens. Through-holes are also etched for the QO fiber and the beam dump. Wafer Si-4 is then bonded to the stack of wafers Si-1 through Si-3.
7. **Fiber Alignment and Bonding:** The QO, DC and FC fibers will either be gold coated or have a gold coated keyed ferrule as in Figure 68. They can be inserted into the keyed hole in the cell and bonded to the silicon wafer using the same Au/Si eutectic bonding as the wafer bonding. The fiber bonding could be done individually by locally heating the metal ferrule or bond all the fibers at once if there is a heating fixture holding all the fibers.

Extension of the Unit Cell and System Alignment

The unit cell as depicted in Figure 68 can be repeated across a silicon wafer to form a larger 2D array of unit cells. This 2D array could be considered one sub-alignment cell of an even larger system by tiling these "wafer size" cells into the larger system. The limitation on the size of the sub cells would be the size of the silicon wafers used and the uniformity of the etching processes across a wafer. Silicon IC facilities today use wafer sizes from 4 to 12 inches in diameter. Each of these sub-alignment cells of the larger system could contain hundreds to thousands of alignment and trap unit cells.

When assembling the larger system, each of the sub-cell alignment cells will need to be aligned to a corresponding trap array. This alignment will have to be done as the trap arrays are tiled together and placed in the vacuum environment. It is envisioned that each of the sub-alignment cells will be tiled into a larger fixture to make up the complete large system and will be grossly aligned to the large trap array in the vacuum environment. The fixturing for each of the wafer size sub-alignment cells will have three-axis and rotation controls for fine alignment of the alignment cell to its corresponding trap array. The fine alignment controls will be vacuum compatible and can be locked down to prevent any movement of the alignment cell after final positioning.

The fine alignment to the trap arrays would be accomplished using photolithographic techniques similar to that used in making integrated circuits or the MEMS structures used in the alignment cells. Alignment marks placed on the trap die array would be aligned to marks on the alignment cell structures. The fine alignment controls are adjusted until the alignment cells are aligned to the trap array and then locked down. Each wafer sized sub-alignment cell would be aligned to the trap arrays in turn until the entire system is aligned.

Detection Cell

The detection cell measures the fluoresced light from each ion position. The detection cell is an array of photo-multiplier tubes (PMTs) to detect the fluoresced photons from the collection fibers, meaning that SMIA enables individual ion detection as well as addressing. A ball lens placed between the fibers and PMTs maximizes the photon detection fidelity. As with the preparation cell, all components of the detection cell are currently commercially available.

4.4 Optical Modeling

The unit cell in Figure 66 was optically modeled using CODEV to test and demonstrate the basic functionality of the alignment cell. CODEV was specifically chosen for this analysis instead of Zemax (or other optical modeling software) because it simulates propagating beams using wavelet analysis, a method that leads to more accurate results for physical optics simulations.

The goal was to show that light from fibers can be coupled to the trapped ion using ball lenses and die mirrors. Only the QO fiber/lens and FC fiber/lens combinations are considered in this section for brevity, similar to Figure 68. Note that the collection ball lens is 2 mm in diameter, and the QO and DC lenses are both 1 mm diameter. The lenses utilize all three dimensions in order to minimize the unit cell volume. With the DC and QO beams spaced 500 μm apart, two

units cells can be paired with a 2 mm length trap. Notice that the QO lens, the lens nearest to the trap, is 3 mm above the trap to accommodate the grounding plane.

The main aspects of the DC and QO beams are the size and location of the beam waists. Figure 69 displays images of the DC and QO beams at the ion location. As desired, the QO beam has a waist of 10 µm and the DC beam a waist of 20 µm ($1/e^2$); thus, the beams are the correct size in the correct location. To quantify the feasibility, a tolerance analysis for the QO beam was performed using CODEV with the results summarized in Table 2 and Table 3. Table 2 displays the modeled tolerances and resulting displacement of the beam waist. The final displacement is calculated using root-sum-squared (RSS), a technique that gives results for the 98th percentile. Here, fairly tight tolerances equate to a beam shift of 6.63 µm. In Table 3, we see that similar relatively tight tolerances equate to a 50 nm change in beam waist.

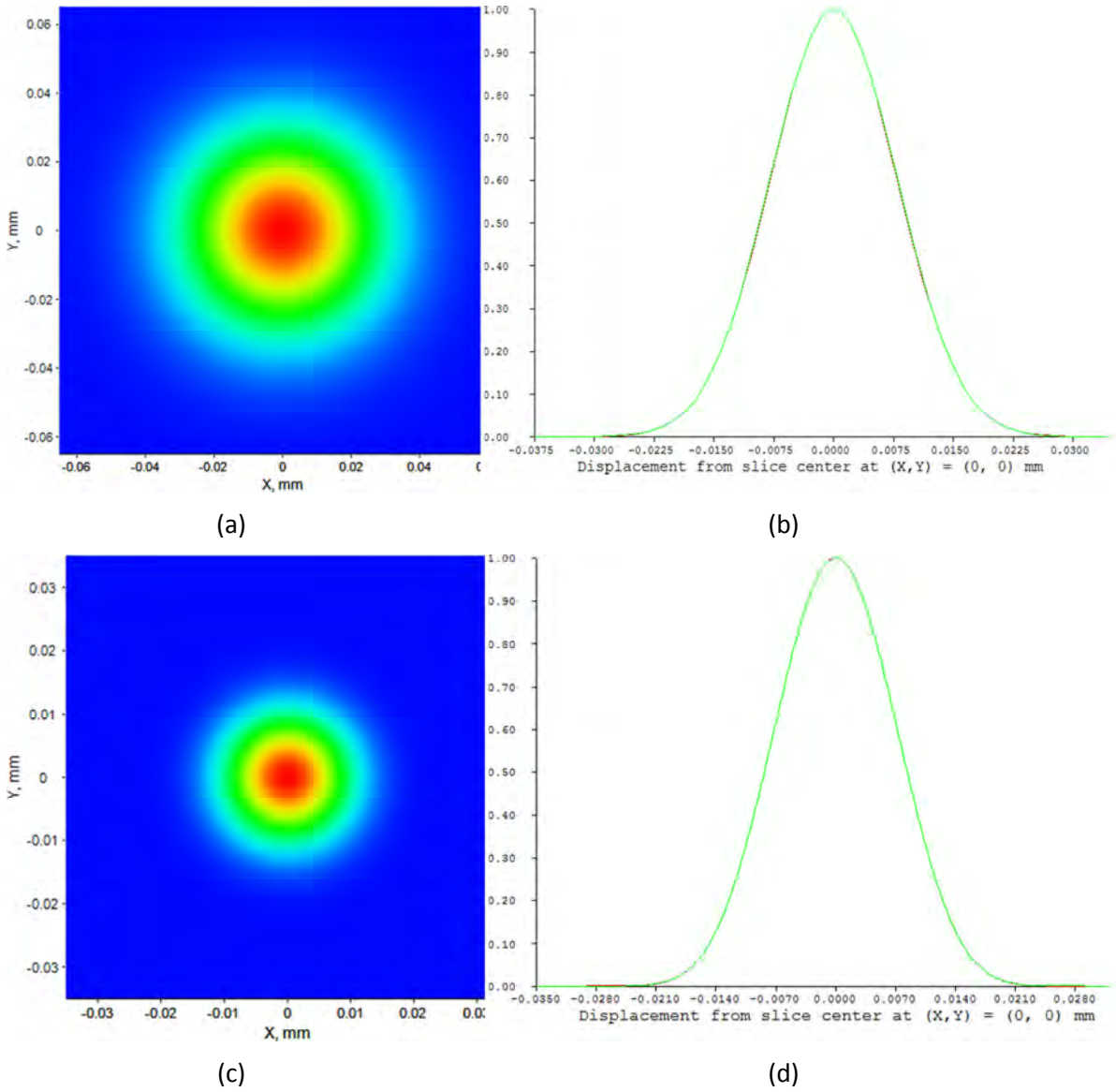


Figure 69: Results of optical modeling: (a) image of DC beam at ion, (b) cross-section of DC beam, (c) image of QO beam at ion, and (d) cross-section of QO beam. Note the difference in scales between the DC and QO beams.

For a 10 µm beam waist, a 50 nm change in waist is only a 0.7% increase, a small change that is unlikely to harm overall performance. A 6.63 µm displacement, however, will likely affect performance since now the ion "sees" roughly a 66% change in beam intensity. The limiting tolerance in Table 2 is the decenter of the fiber and ball lens combination to the fold mirror. This factor is caused by the large ratio between the lens-to-ion distance and the fiber-to-lens distance; thus, this tolerance can be greatly mitigated by increasing the fiber to ball lens distance. Other tolerances can also be decreased with improved manufacturing techniques or active alignment control, although both solutions could possibly require a shift in the current state-of-the-art. Therefore, the alignment of the alignment cell is a significant challenge moving forward.

Parameter	Tolerance	Sensitivity	Displacement (µm)
Fiber to ball decenter	1.0 µm	1.00 (µm/µm)	1.00
Fiber/ball combination decenter to fold mirror	1.0 µm	6.45 (µm/µm)	6.45
Fold mirror angle	0.6 arcmin	83.3 (µm/deg)	0.83
Fold mirror orientation	0.6 arcmin	83.3 (µm/deg)	0.83
	RSS Waist Displacement (µm)		**6.63**

Table 2: Results of QO tolerancing analysis for displacement of beam at ion. The final waist displacement is calculated using root-sum-squared (RSS).

Parameter	Tolerance (µm)	Sensitivity (µm/µm)	Displacement (µm)
Fiber to ball lens defocus	25	0.0028	0.07
Fiber/ball combination defocus	250	0.00028	0.07
Ball diameter	5	0.00125	0.00625
Ball refractive index	0.005	4	0.02
		RSS Waist Change (µm)	**0.05**

Table 3: Results of QO tolerancing analysis for change in beam waist at ion. The final waist change is calculated using root-sum-squared (RSS).

The final aspect of the alignment cell is the collection of fluoresced light. Figure 68 displays the simplified geometry for the fluorescence modeling with the micromirror placed directly below the ion. Building upon the aforementioned paper, the micromirror's numerical aperture (NA) was set to 0.8; notice that the mirror's focal length is such that the "downward" fluoresced light is collimated. Then, the collection ball lens will gather some of the "upward" fluoresced light

with an NA = 0.2. The combination of these cone angles results in an overall collection efficiency of 21%.

4.5 Summary

Scalable Multiplexors for single-Ion Addressing (SMIA) addresses the need for scalability in ion trap technology by splitting the required structure into three cells. Two cells split a single laser into many beams, where each beam can have a different frequency, polarization state, and intensity to allow for single ion addressing. The third cell collects and measures the fluoresced light to also allow for single ion detecting. SMIA fills extra space on the die surface with flat mirrors that deliver light to the ion, and utilizes a micromirror placed under the ion to increase collection efficiency. Also, SMIA employs off-the-shelf components and understood MEMS fabrication techniques, albeit in novel combinations. Finally, optical modeling shows that the desired beam waists of 10 µm and 20 µm (for the qubit operation and Doppler cooling beams, respectively) can be garnered with very tight tolerances, and that SMIA collects fluoresced light with an efficiency of 21%.

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